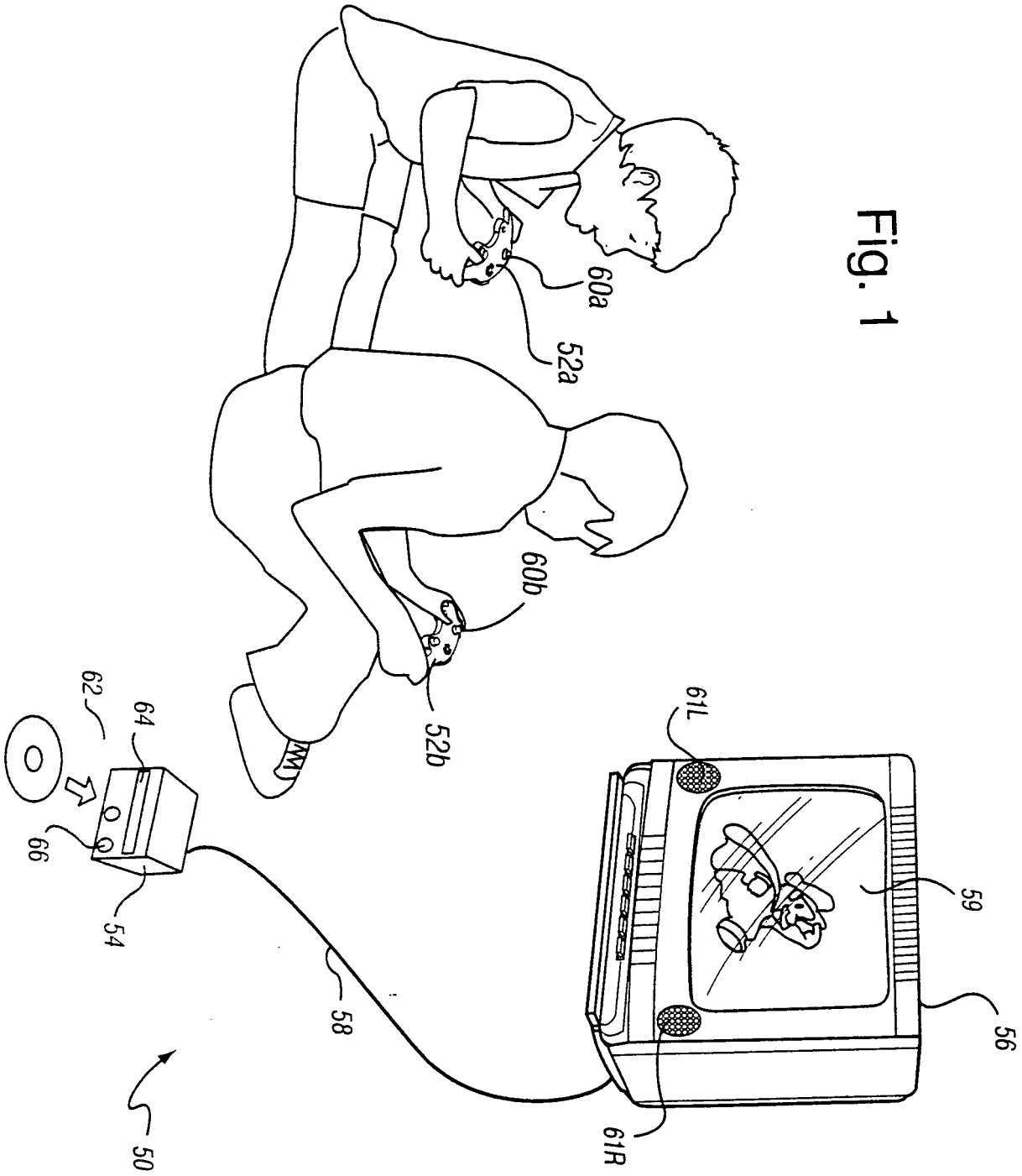



Fig. 1

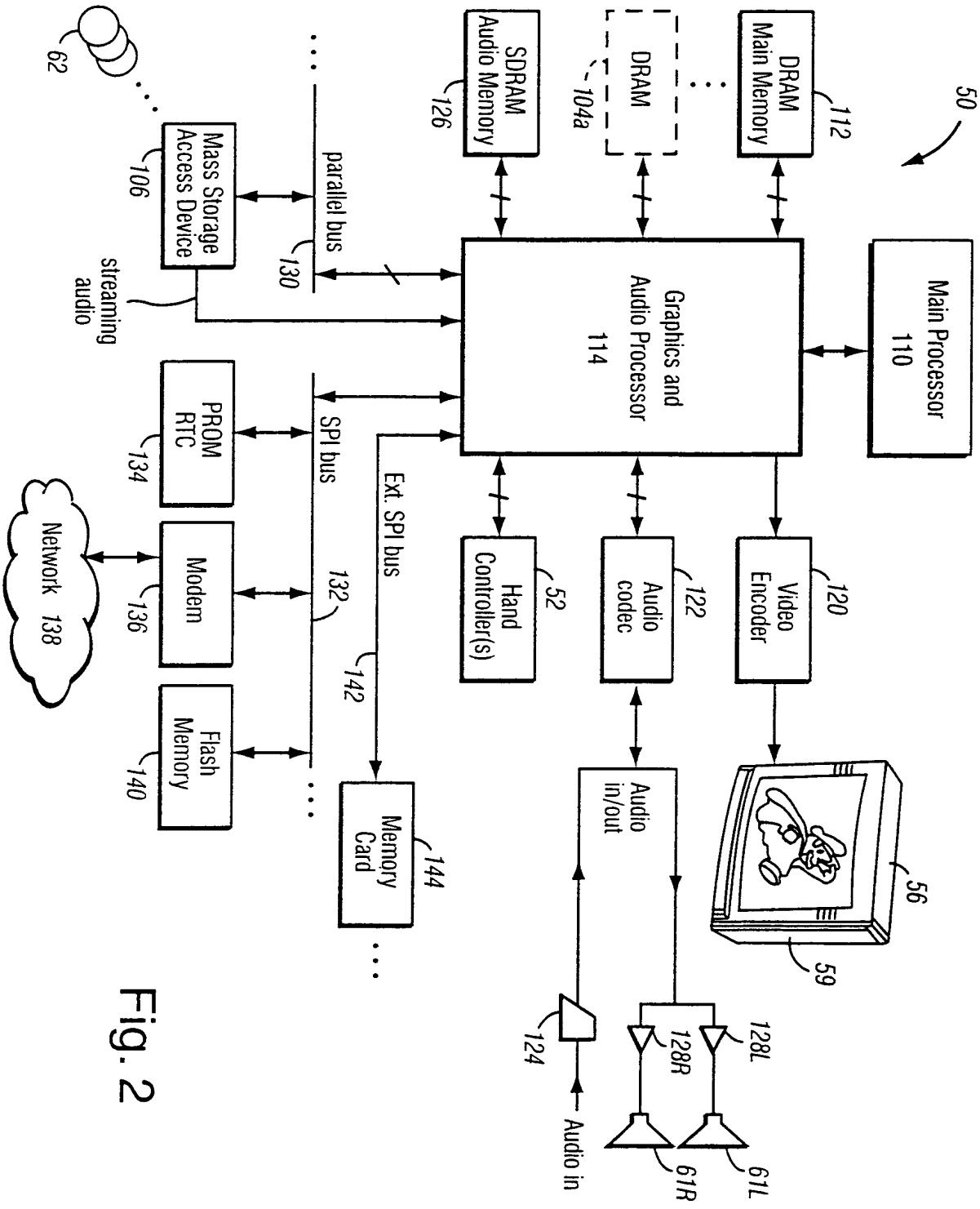

50
DRAM Main Memory
112
DRAM
104a
SDRAM Audio Memory
126
Main Processor 110
Graphics and Audio Processor 114
Video Encoder
120
Audio codec
122
Hand Controller(s)
52
56
59
Audio in/out
124
128L
128R
61L
61R
Audio in
62
Mass Storage Access Device
106
parallel bus
130
streaming audio
PROM RTC
134
SPI bus
132
Ext. SPI bus
142
Modem
136
Network 138
Flash Memory
140
Memory Card
144

Fig. 2

Fig. 3

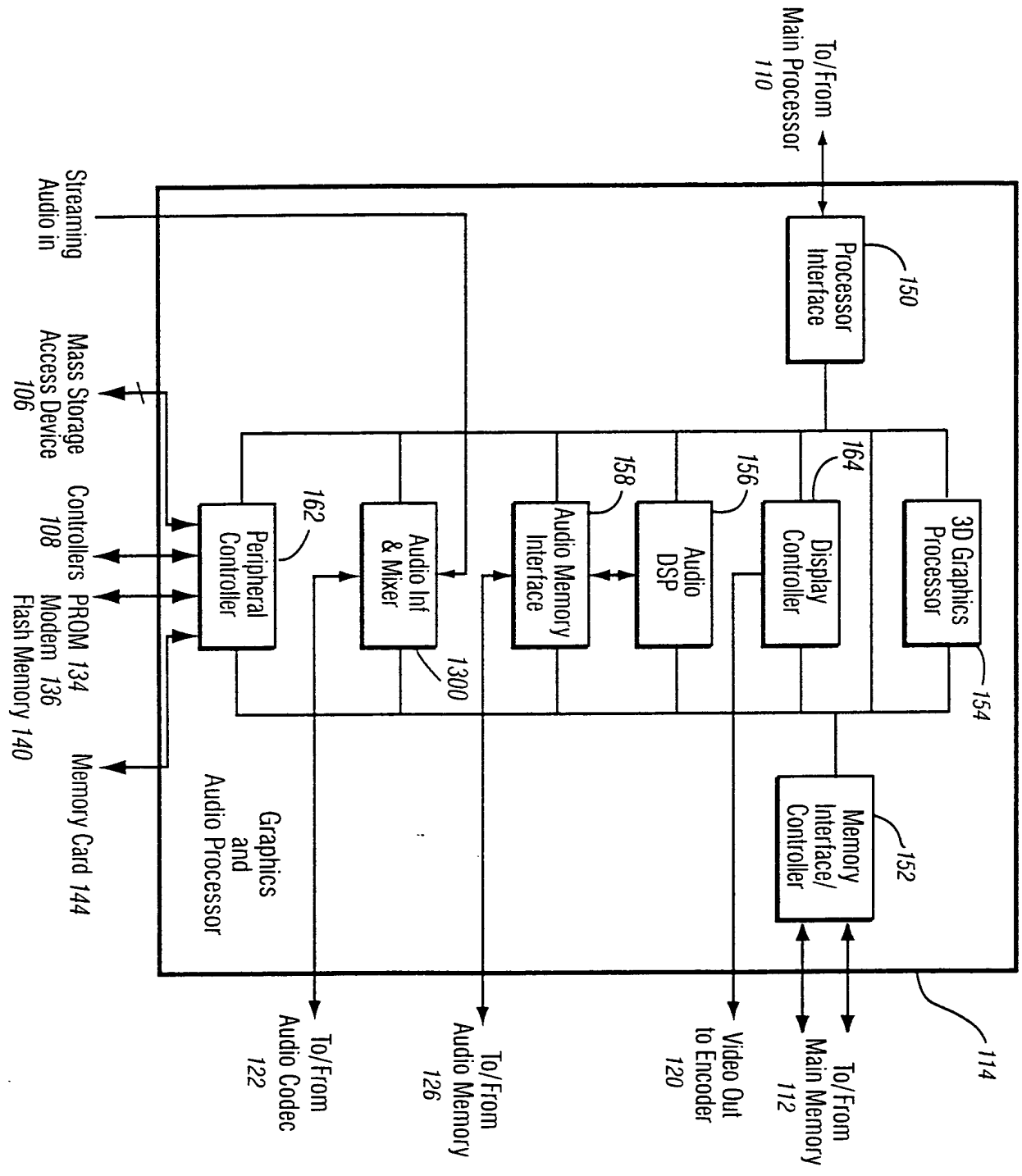
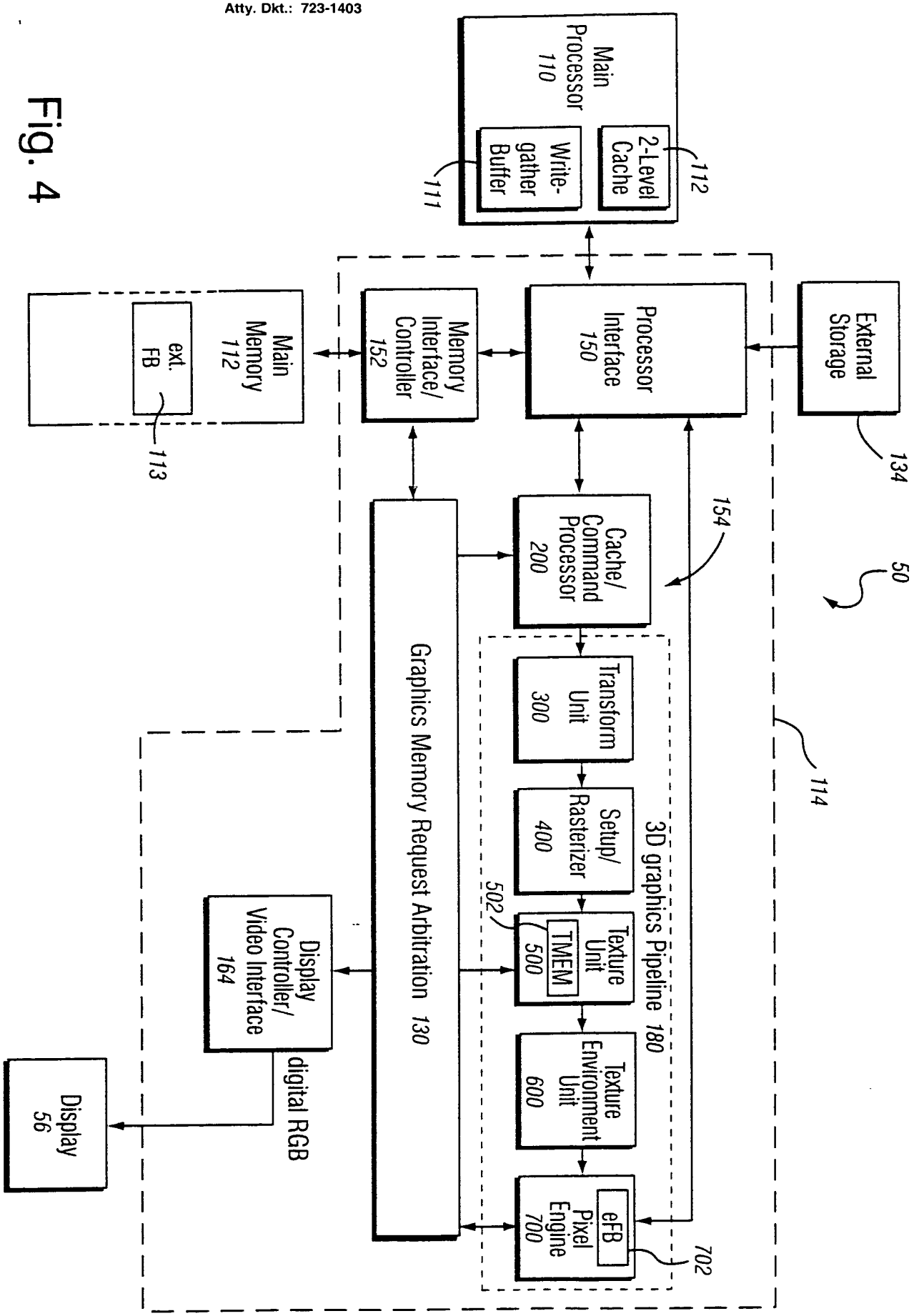

To/From Main Processor 110
Processor Interface 150
3D Graphics Processor 154
Display Controller 164
Audio DSP 156
Audio Memory Interface 158
Audio Int & Mixer 1300
Peripheral Controller 162
Memory Interface/ Controller 152
Graphics and Audio Processor
Streaming Audio in
Mass Storage Access Device 106
Controllers 108
PROM 134
Modem 136
Flash Memory 140
Memory Card 144
114
To/From Main Memory 112
Video Out to Encoder 120
To/From Audio Memory 126
To/From Audio Codec 122

Fig. 4


Main Processor 110
2-Level Cache 112
Write-gather Buffer 111
External Storage
134
Processor Interface 150
Memory Interface/ Controller 152
Main Memory 112
ext. FB 113
50
154
Cache/ Command Processor 200
Graphics Memory Request Arbitration 130
3D graphics Pipeline 180
114
Transform Unit 300
Setup/ Rasterizer 400
502
Texture Unit 500
TMEM
Texture Environment Unit 600
Pixel Engine 700
eFB
702
Display Controller/ Video Interface 164
digital RGB
Display 56

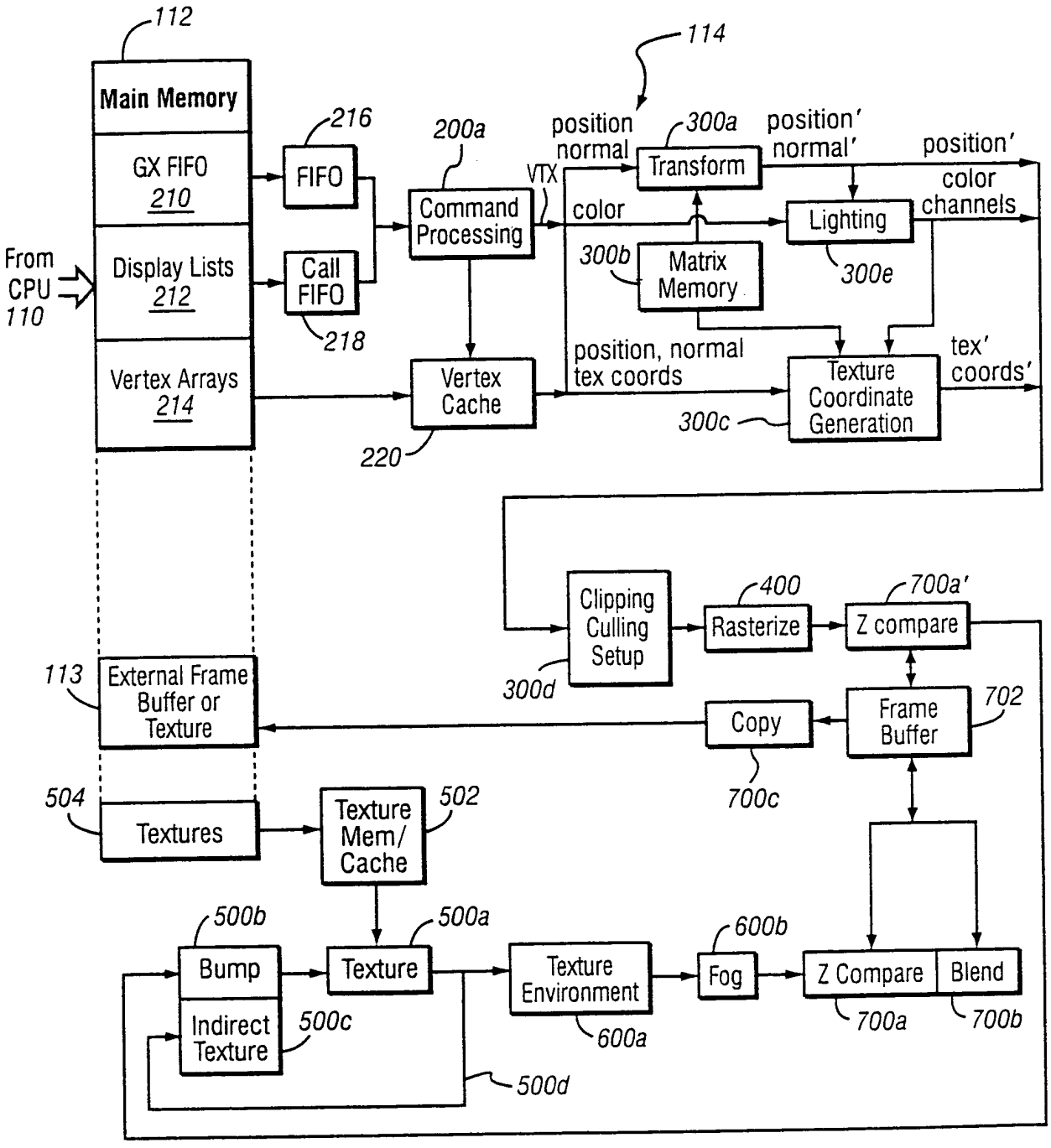
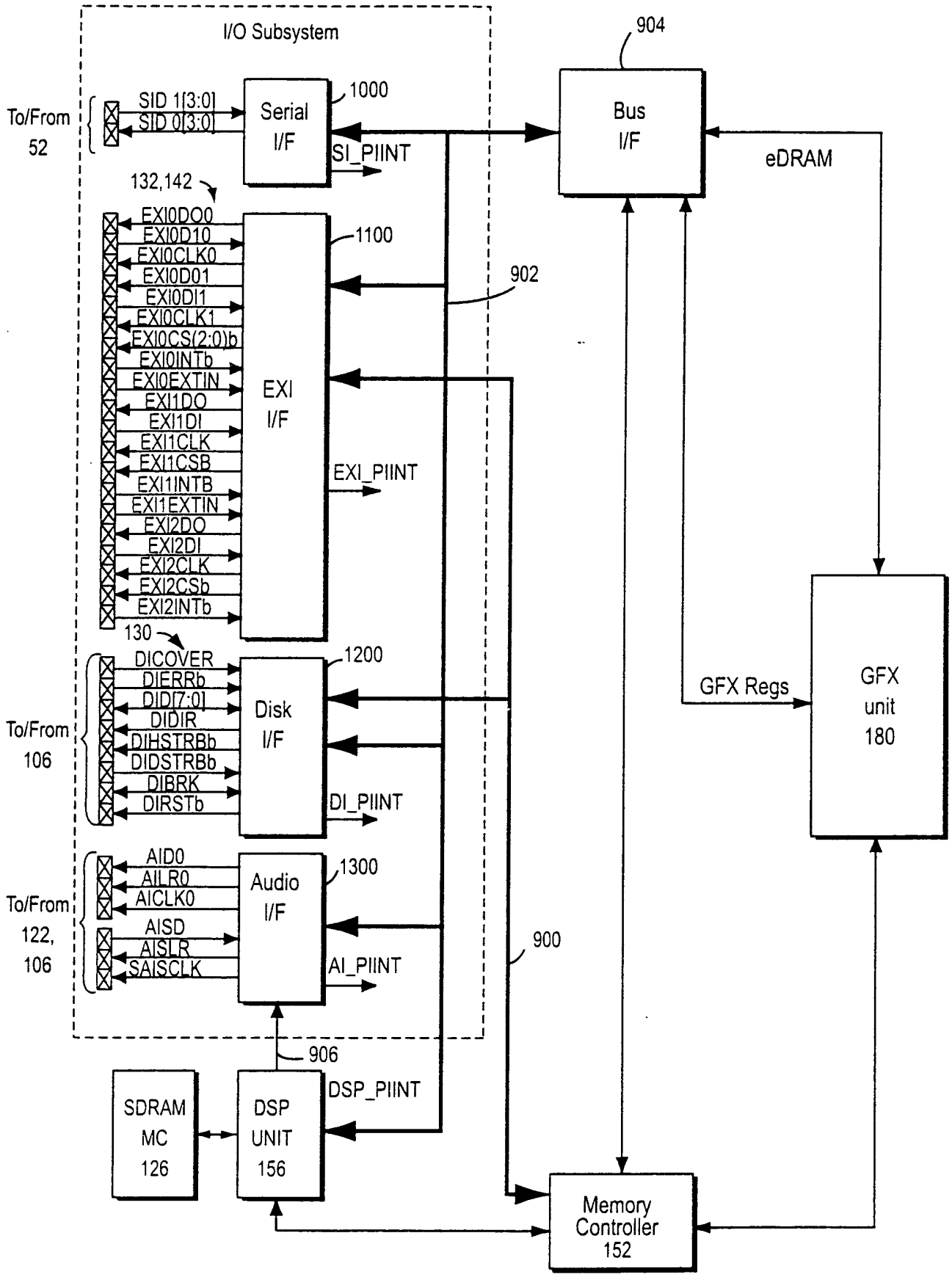



Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

# Fig. 6 EXAMPLE INPUT/OUTPUT SUBSYSTEM



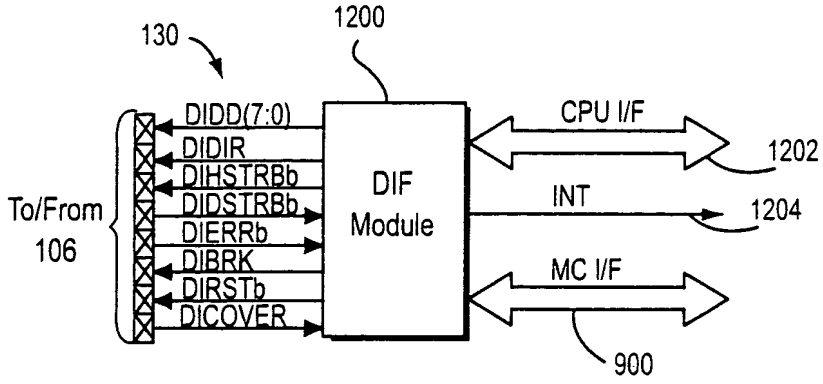



Fig. 7A
EXAMPLE DISK INTERFACE

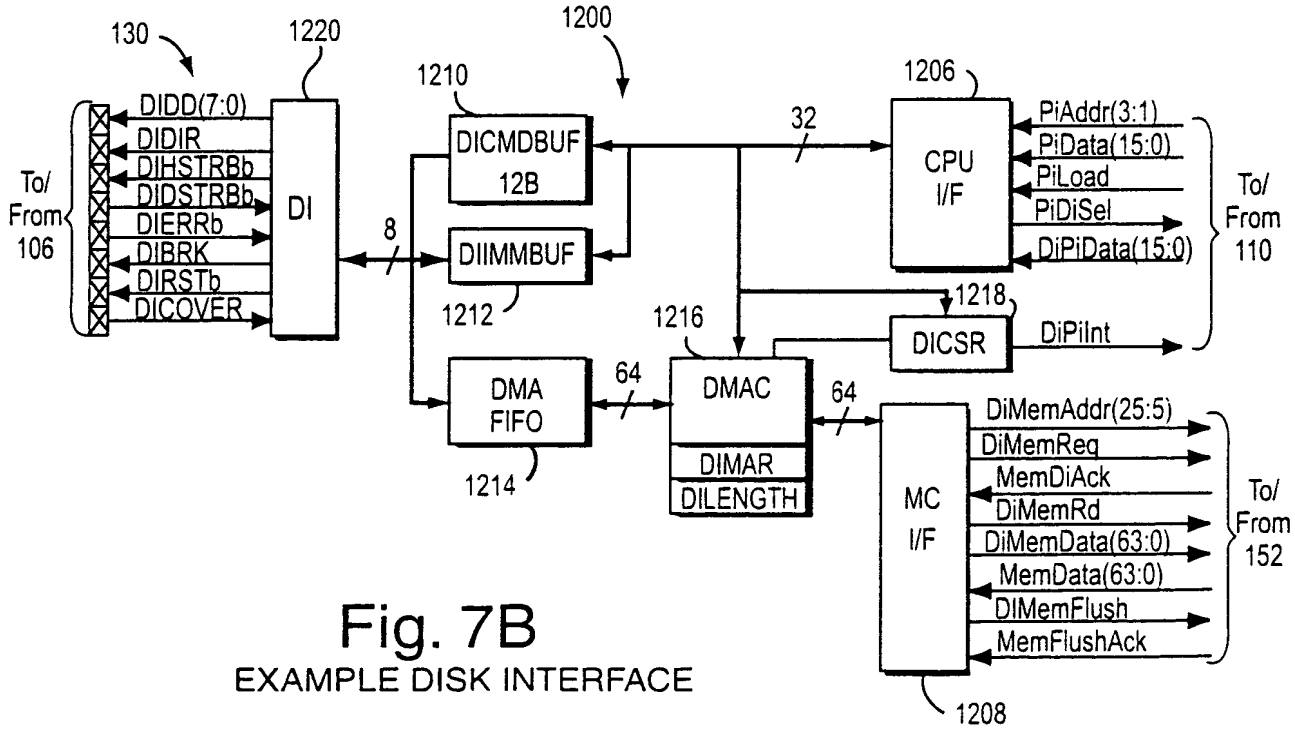



Fig. 7B
EXAMPLE DISK INTERFACE

| Register | | | | Offset(hex) |
|---|---|---|---|---|
| 31 | 16 | 15 | 0 | |
| DI Status Register (DISR) | | | | 0x00 |
| DI Cover Register (DICCVR) | | | | 0x04 |
| DI Command Buffer 0 (DICMDBUF0) | | | | 0x08 |
| DI Command Buffer 1 (DICMDBUF1) | | | | 0x0C |
| DI Command Buffer 2 (DICMDBUF2) | | | | 0x10 |
| DI Memory Address Register (DIMAR) | | | | 0x14 |
| DI DMA Length Register (DILENGTH) | | | | 0x18 |
| DI Control Register (DICR) | | | | 0x1C |
| DI Immediate Data Buffer (DIMMBUF) | | | | 0x20 |
| DI Configuration Register (DICFG) | | | | 0x24 |

Fig. 7C

EXAMPLE DISK INTERFACE REGISTERS

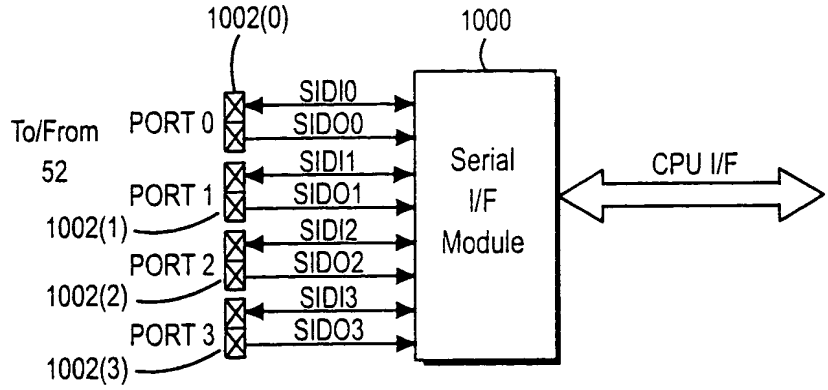



Fig. 8A
EXAMPLE SERIAL INTERFACE

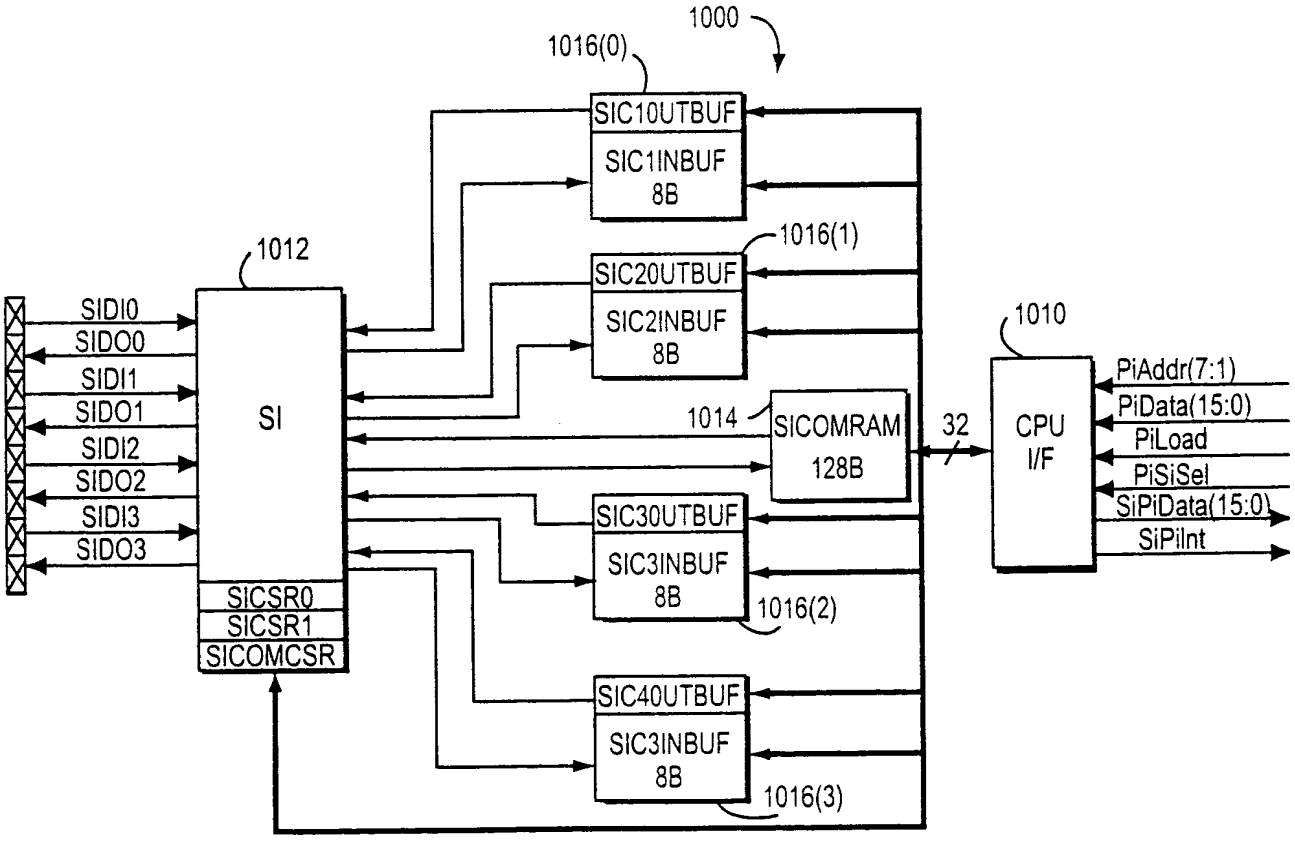



Fig. 8B
EXAMPLE SERIAL INTERFACE

| Register | | | Offset(hex) |
|---|---|---|---|
| 31 | 16 \| 15 | 0 | |
| SI Channel 0 Output Buffer (SIC0OUTBUF) | | | 0x00 |
| SI Channel 0 Output Buffer H(SIC0INBUFH) | | | 0x04 |
| SI Channel 0 Output Buffer L(SIC0INBUFL) | | | 0x08 |
| SI Channel 1 Output Buffer (SIC1OUTBUF) | | | 0x0C |
| SI Channel 1 Input Buffer H(SIC1INBUFH) | | | 0x10 |
| SI Channel 1 Input Buffer L(SIC1INBUFL) | | | 0x14 |
| SI Channel 2 Output Buffer (SIC2OUTBUF) | | | 0x18 |
| SI Channel 2 Input Buffer H(SIC2INBUFH) | | | 0x1C |
| SI Channel 2 Input Buffer L(SIC2INBUFL) | | | 0x20 |
| SI Channel 3 Output Buffer (SIC3OUTBUF) | | | 0x24 |
| SI Channel 3 Input Buffer H(SIC3INBUFH) | | | 0x28 |
| SI Channel 3 Input Buffer L(SIC3INBUFL) | | | 0x2C |
| SI Poll Control Register (SIPOLL) | | | 0x30 |
| SI Communication Control Status Register (SICOMCSR) | | | 0x34 |
| SI Status Register (SISR) | | | 0x38 |
| SI EXI Lock Register (SIEXILK) | | | 0x3C |
| SI Communication RAM (128 Bytes) | | | 0x80-0xFF |

Fig. 8C

EXAMPLE SERIAL INTERFACE REGISTERS

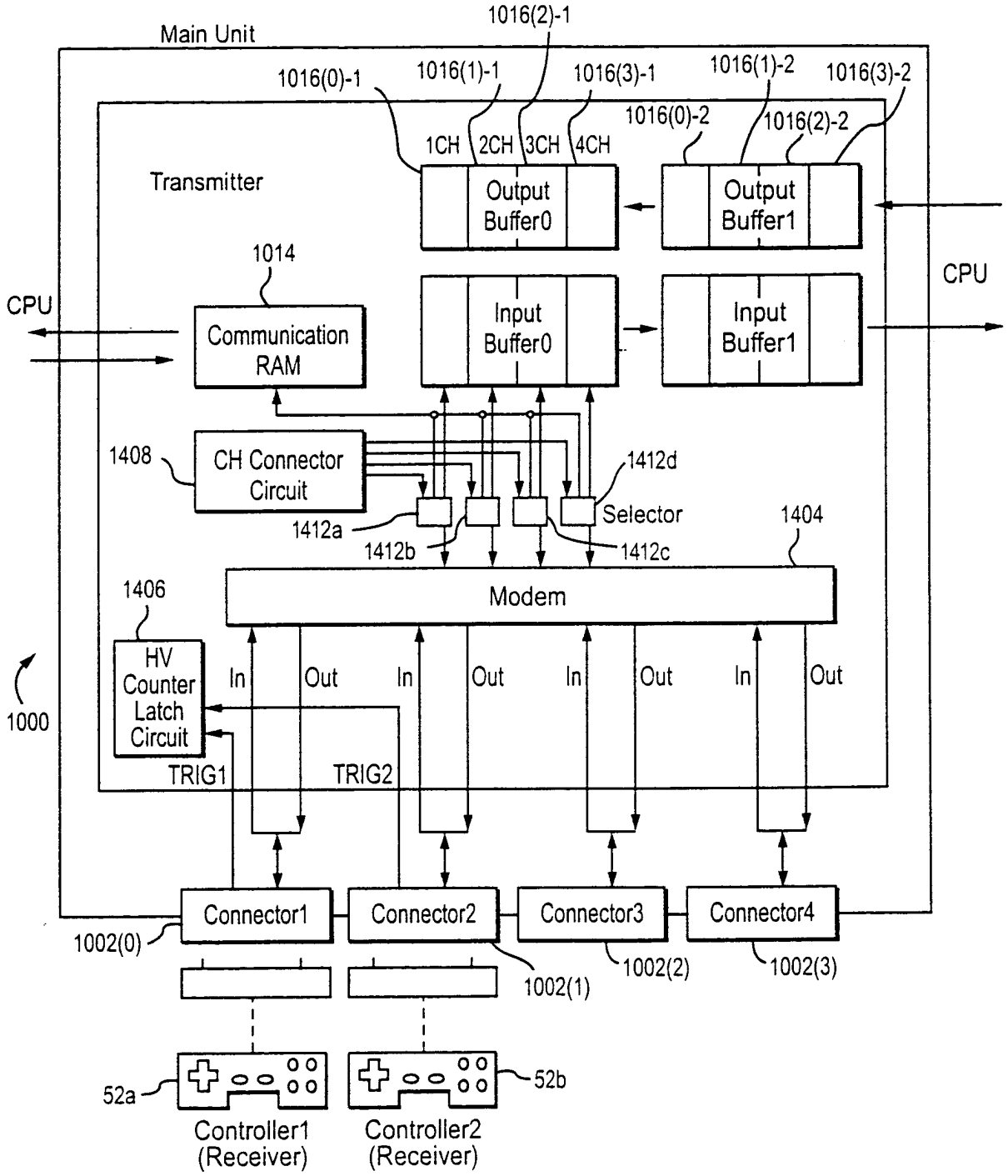



Fig. 8D

EXAMPLE SERIAL INTERFACE

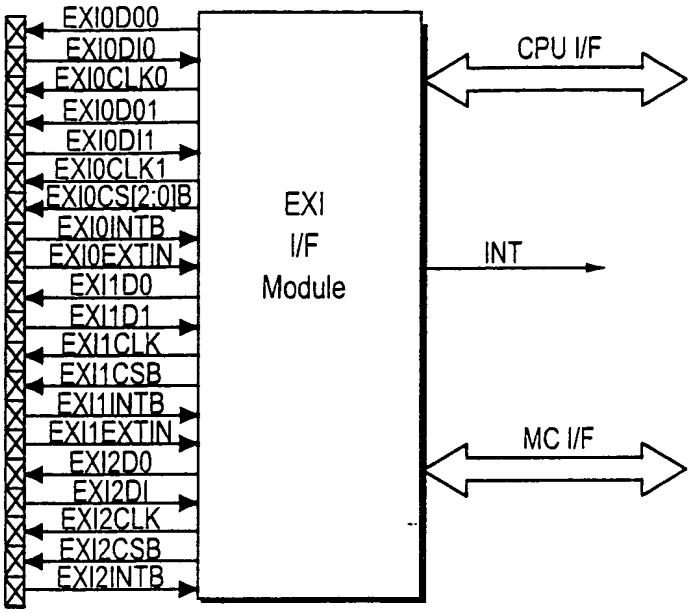



Fig. 9A

EXAMPLE EXTERNAL INTERFACE

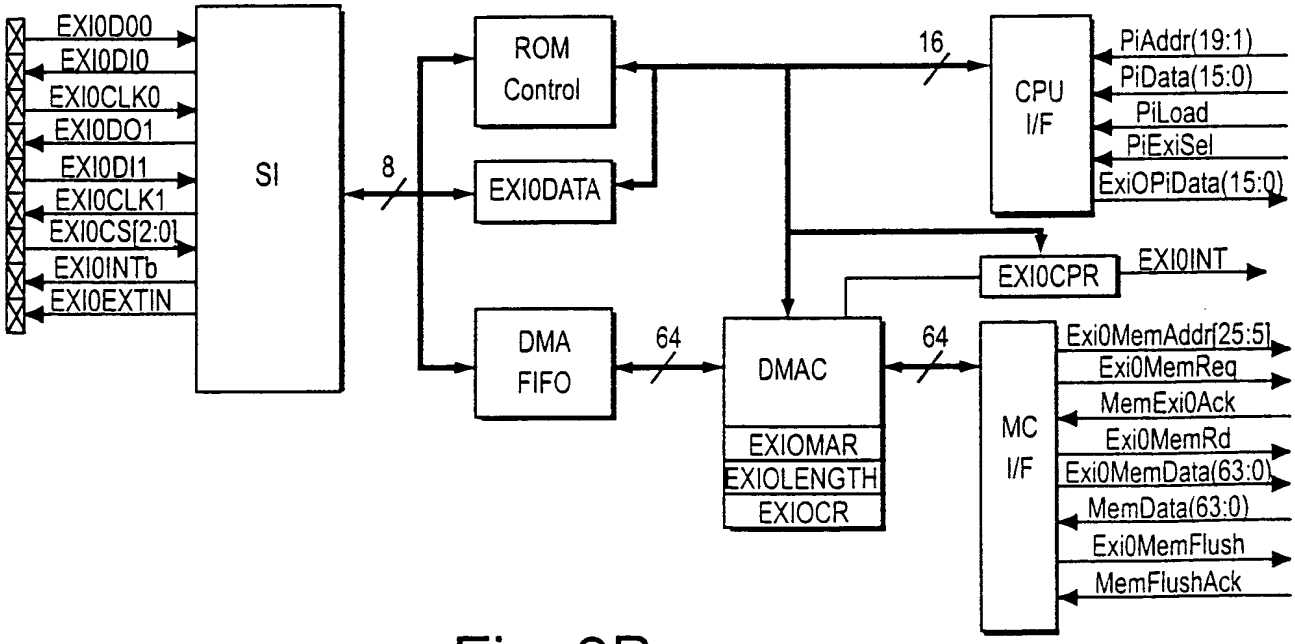



Fig. 9B

EXAMPLE EXTERNAL CHANNEL Ø INTERFACE

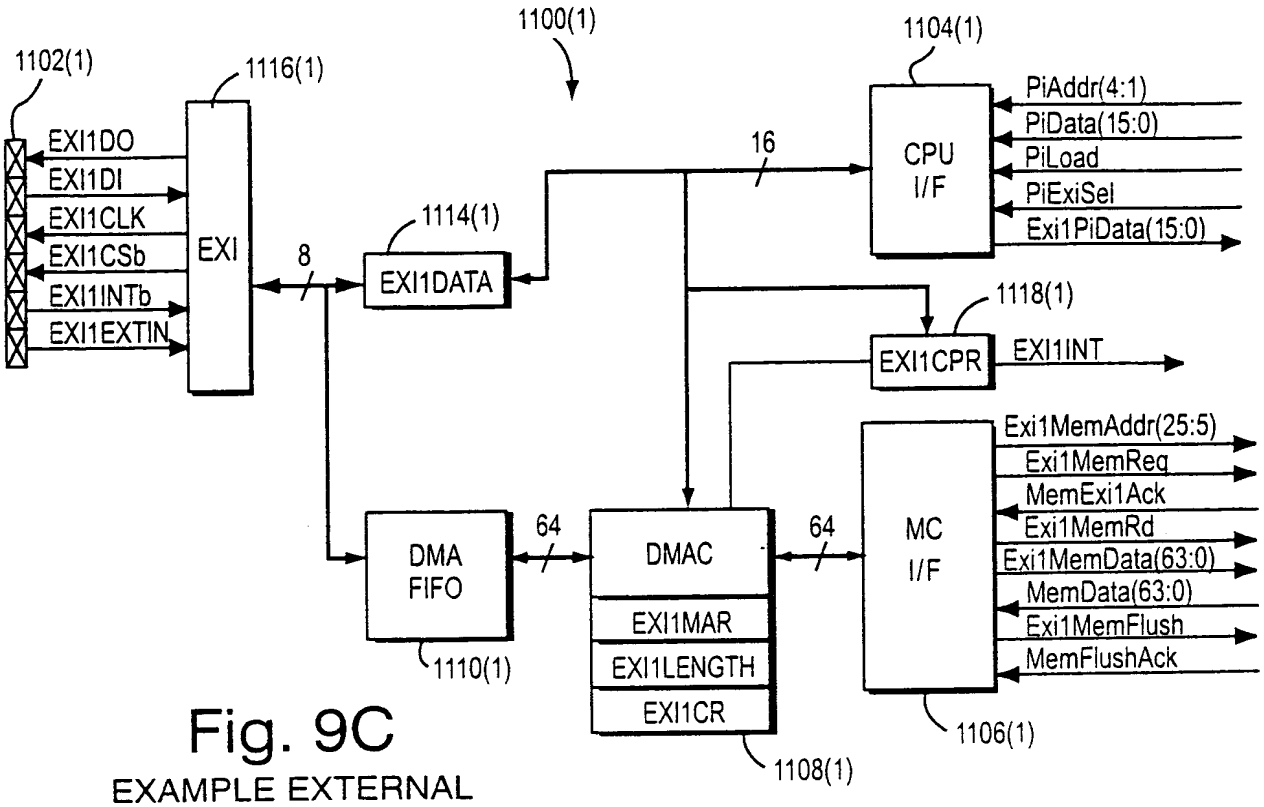



Fig. 9C
EXAMPLE EXTERNAL
CHANNEL 1 INTERFACE

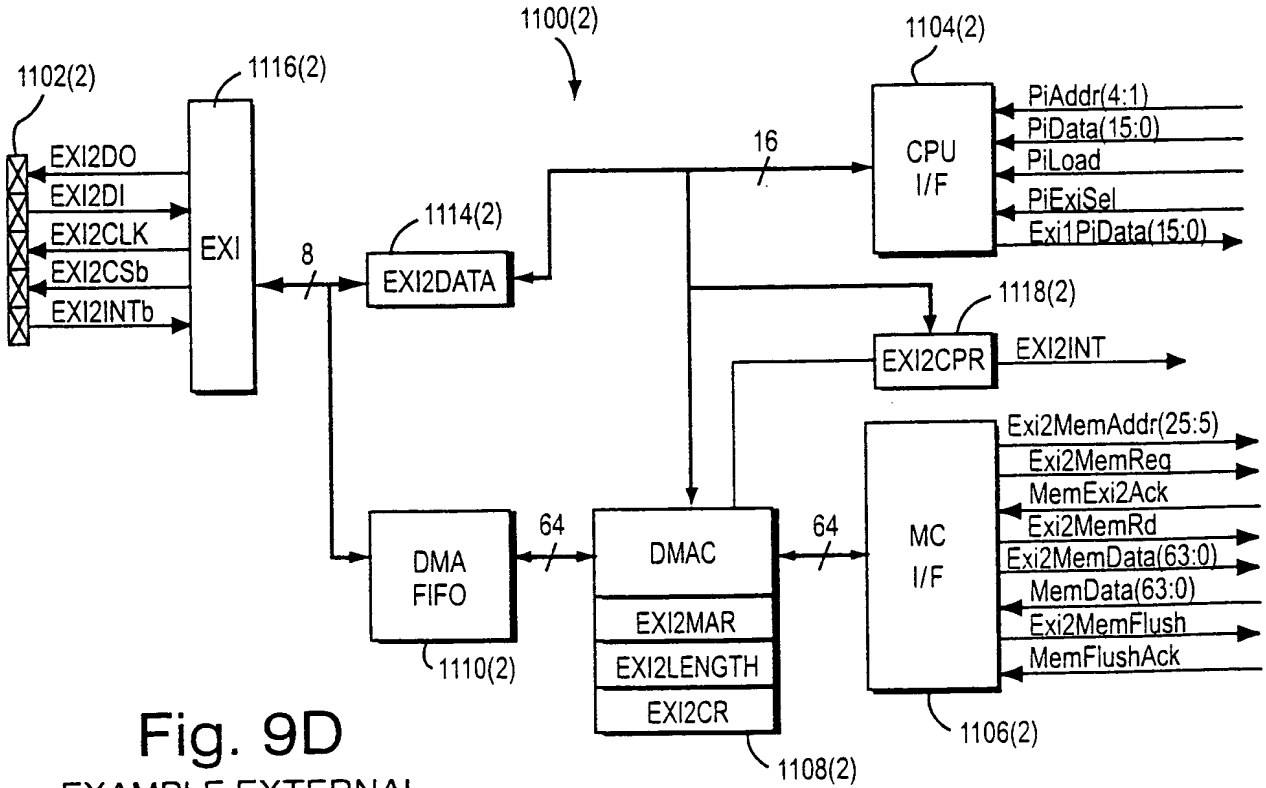



Fig. 9D
EXAMPLE EXTERNAL
CHANNEL 2 INTERFACE

| Register | | | | Offset(hex) |
|---|---|---|---|---|
| 31 | 16 | 15 | 0 | |
| EXI0 Channel Parameter Register (EXI0CPR) | | | | 0x00 |
| EXI0 Memory Address Register (EXI0MAR) | | | | 0x04 |
| EXI0 DMA Length (EXI0LENGTH) | | | | 0x08 |
| EXI0 Control Register (EXI0CR) | | | | 0x0C |
| EXI0 Data Register (EXI0DATA) | | | | 0x10 |
| EXI1 Channel Parameter Register (EXI1CPR) | | | | 0x14 |
| EXI1 Memory Address Register (EXI1MAR) | | | | 0x18 |
| EXI1 DMA Length (EXI1LENGTH) | | | | 0x1C |
| EXI1 Control Register (EXI1CR) | | | | 0x20 |
| EXI1 Data Register (EXI1DATA) | | | | 0x24 |
| EXI2 Channel Parameter Register (EXI2CPR) | | | | 0x28 |
| EXI2 Memory Address Register (EXI2MAR) | | | | 0x2C |
| EXI2 DMA Length (EXI2LENGTH) | | | | 0x30 |
| EXI2 Control Register (EXI2CR) | | | | 0x34 |
| EXI2 Data Register (EXI2DATA) | | | | 0x38 |
| ROM Area (1MB) | | | | 0xFFF00000 |

Fig. 9E

EXAMPLE EXTERNAL INTERFACE REGISTERS

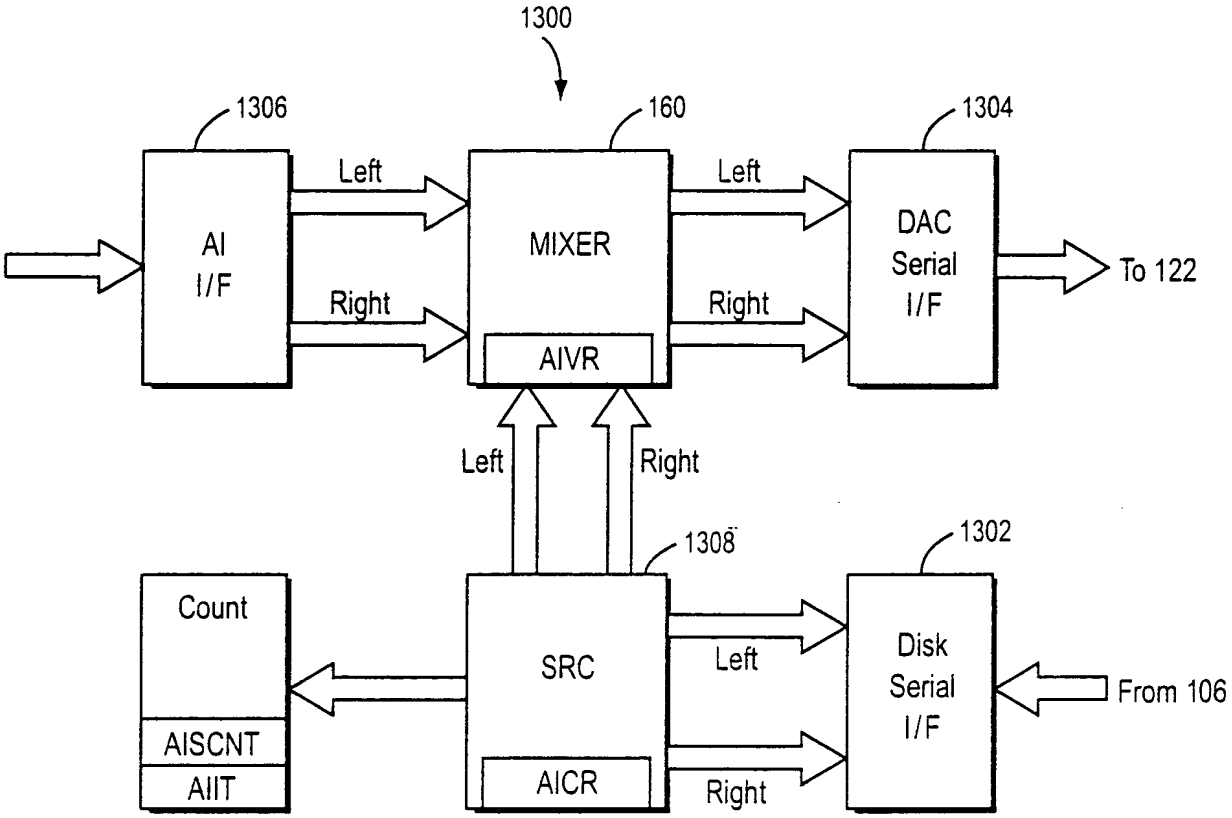



Fig. 10A
EXAMPLE AUDIO INTERFACES

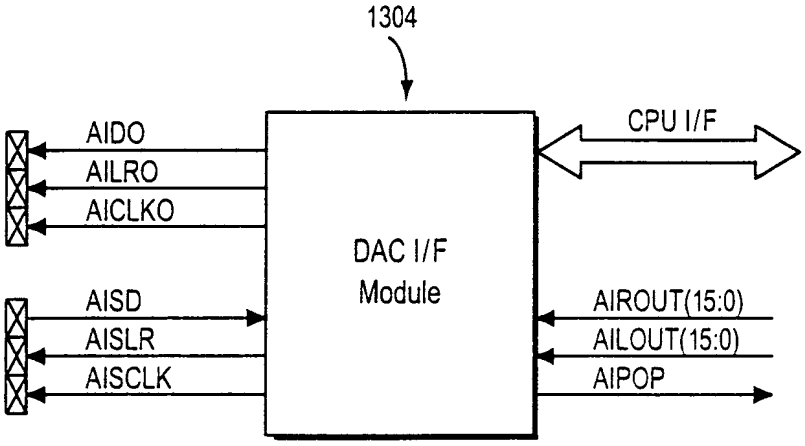



Fig. 10B
EXAMPLE AUDIO DAC INTERFACES

| Register | | | | Offset(hex) |
|---|---|---|---|---|
| 31 | 16 | 15 | 0 | |
| AI Control Register (AICR) | | | | 0x00 |
| AI Volume Register (AIVR) | | | | 0x04 |
| AI Sample Count Register (AISCNT) | | | | 0x08 |
| AI Interrupt Timing Register (AIIT) | | | | 0x0C |

Fig. 10C

EXAMPLE AUDIO INTERFACES REGISTERS

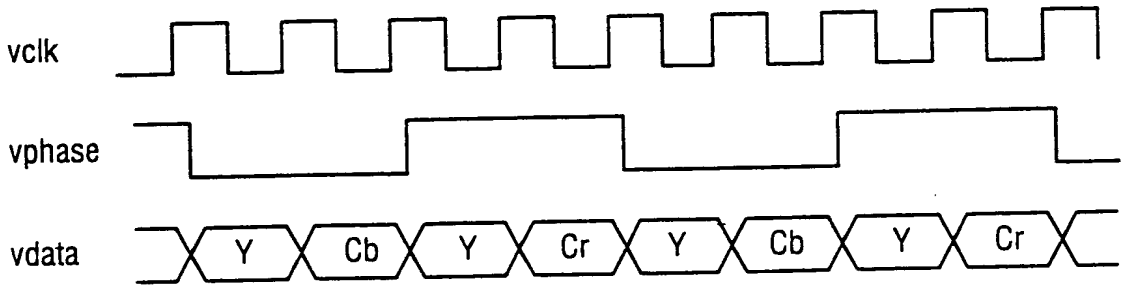



Fig. 11A

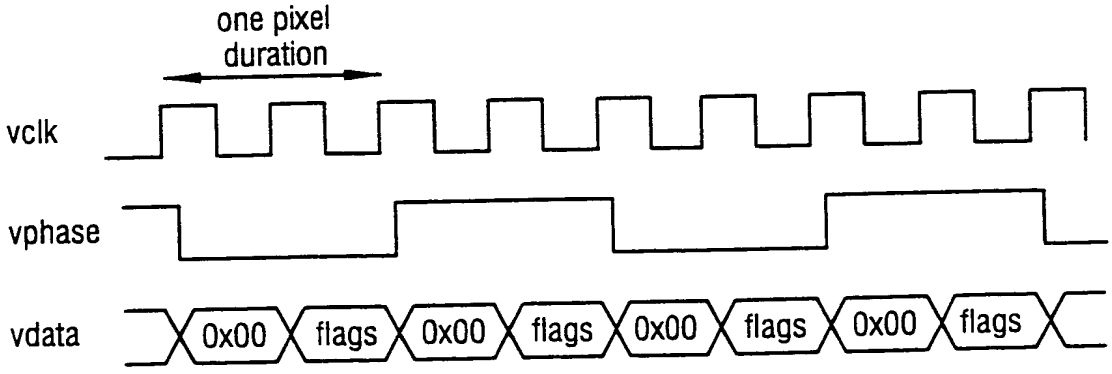



Fig. 11B

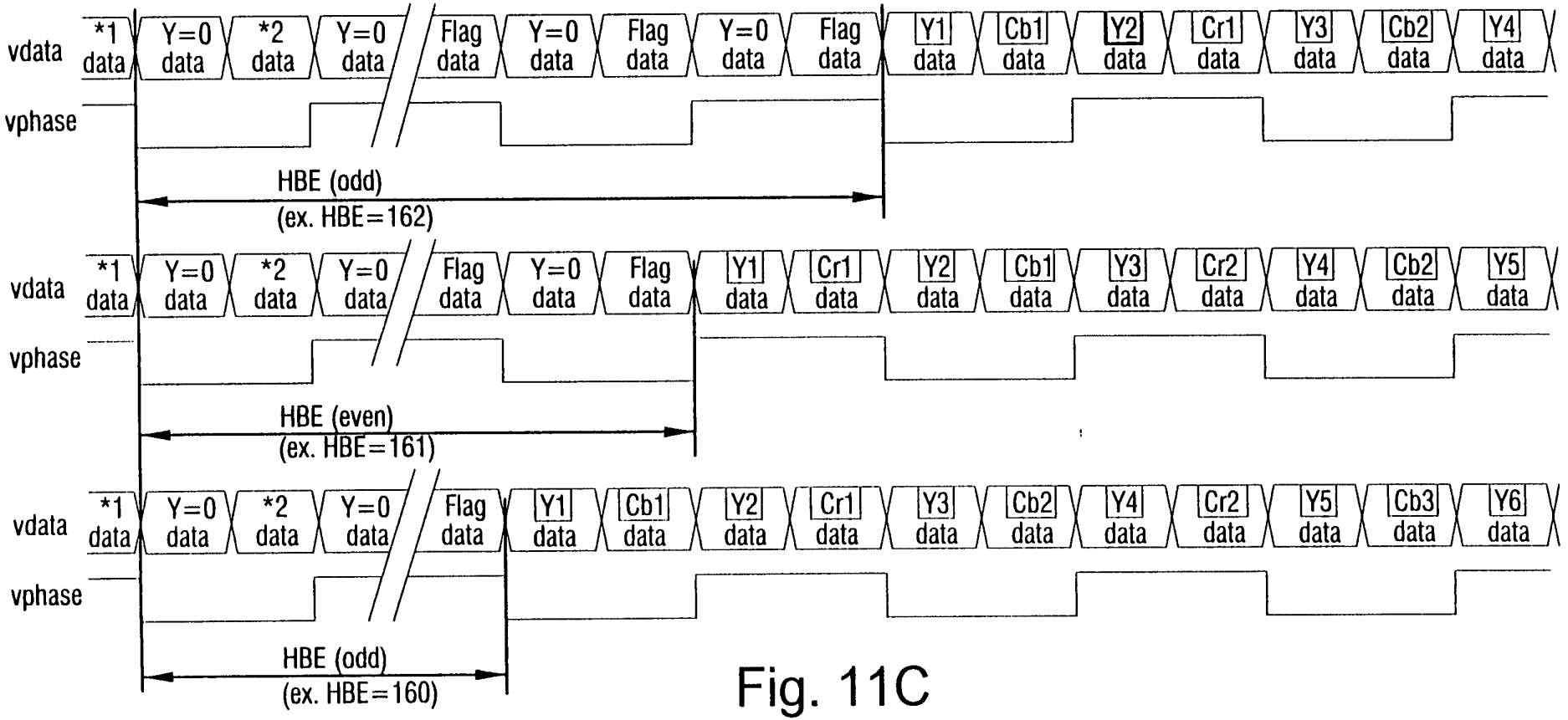

vdata
*1 data
Y=0 data
*2 data
Y=0 data
Flag data
Y=0 data
Flag data
Y=0 data
Flag data
Y1 data
Cb1 data
Y2 data
Cr1 data
Y3 data
Cb2 data
Y4 data
vphase
HBE (odd)
(ex. HBE=162)
vdata
*1 data
Y=0 data
*2 data
Y=0 data
Flag data
Y=0 data
Flag data
Y1 data
Cr1 data
Y2 data
Cb1 data
Y3 data
Cr2 data
Y4 data
Cb2 data
Y5 data
vphase
HBE (even)
(ex. HBE=161)
vdata
*1 data
Y=0 data
*2 data
Y=0 data
Flag data
Y1 data
Cb1 data
Y2 data
Cr1 data
Y3 data
Cb2 data
Y4 data
Cr2 data
Y5 data
Cb3 data
Y6 data
vphase
HBE (odd)
(ex. HBE=160)

Fig. 11C

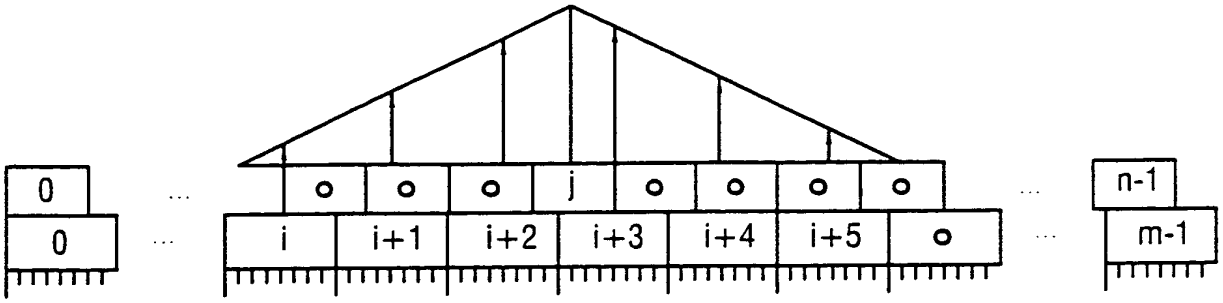



Fig. 11D

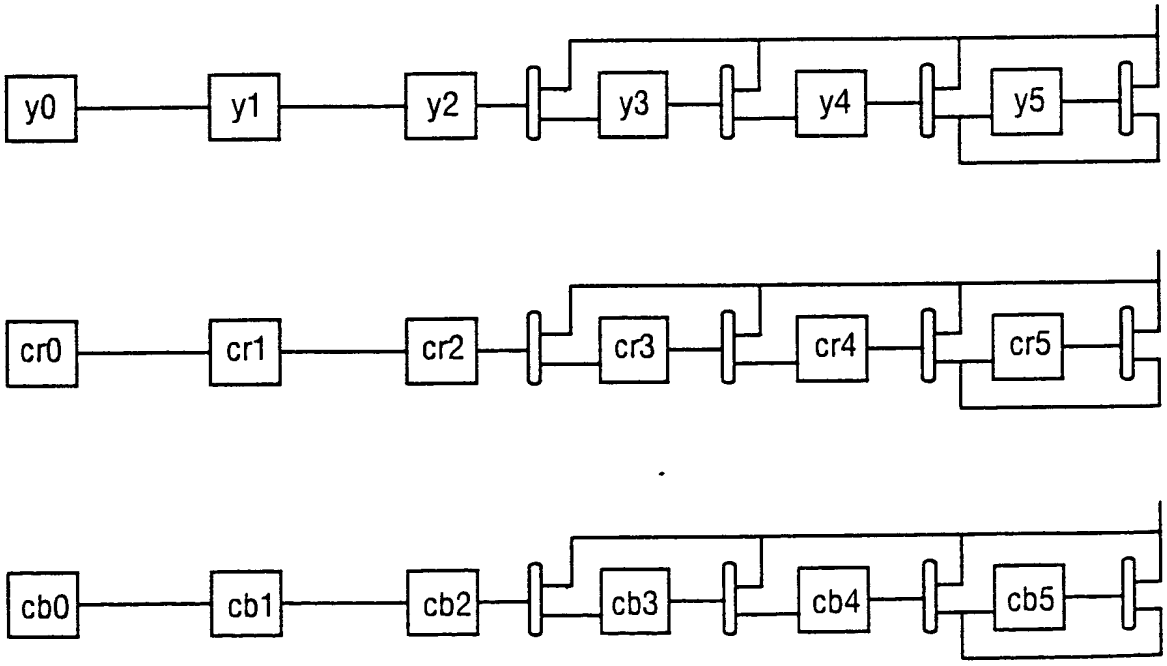



Fig. 11E

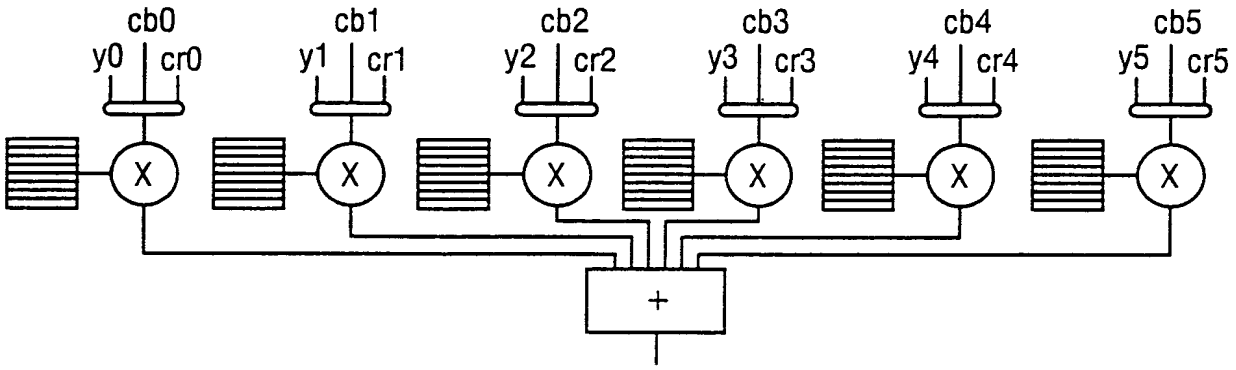



Fig. 11F

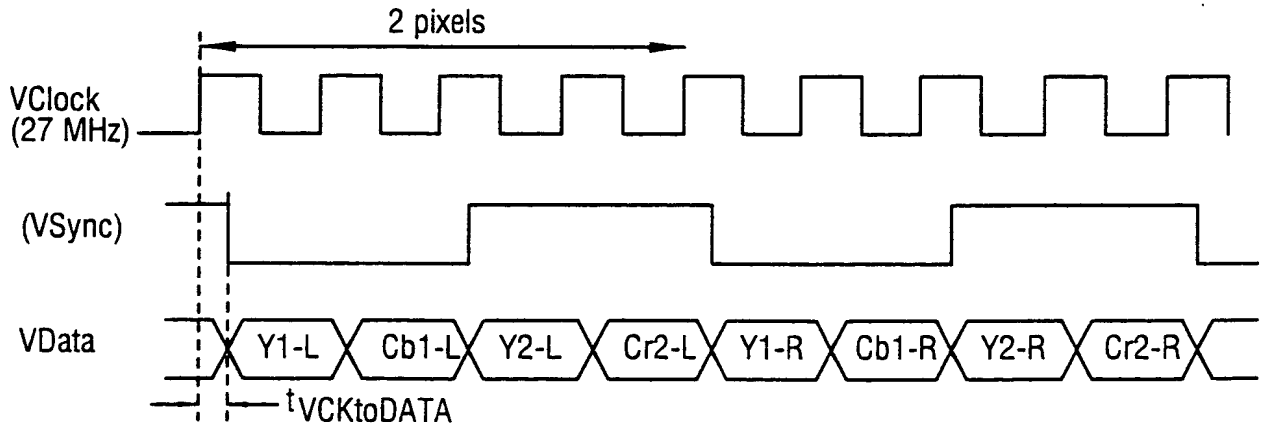



Fig. 11G

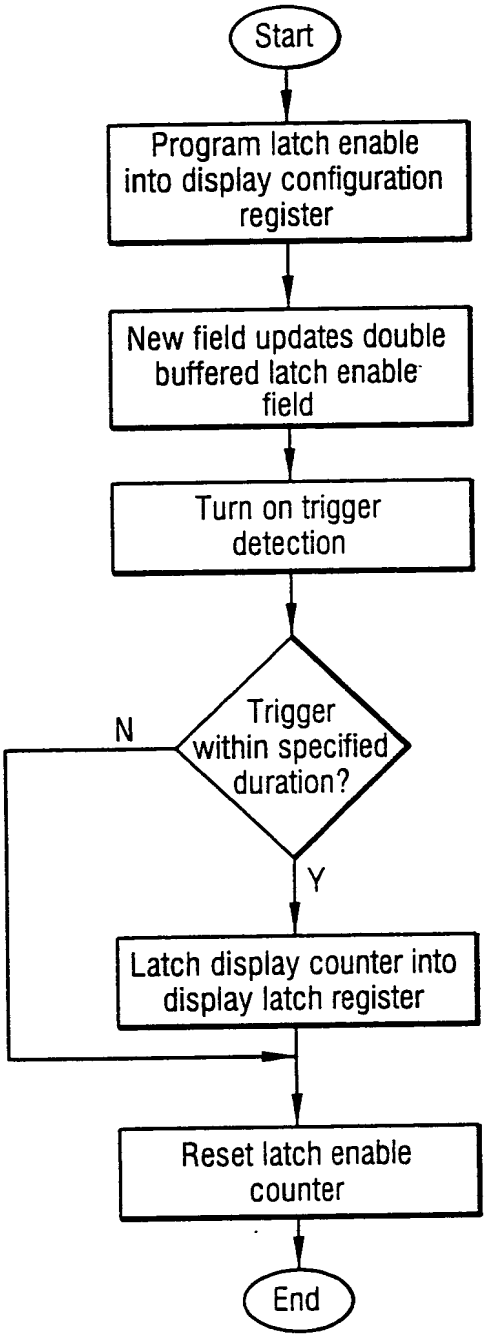

Start
Program latch enable into display configuration register
New field updates double buffered latch enable field
Turn on trigger detection
Trigger within specified duration?
N
Y
Latch display counter into display latch register
Reset latch enable counter
End

Fig. 11H

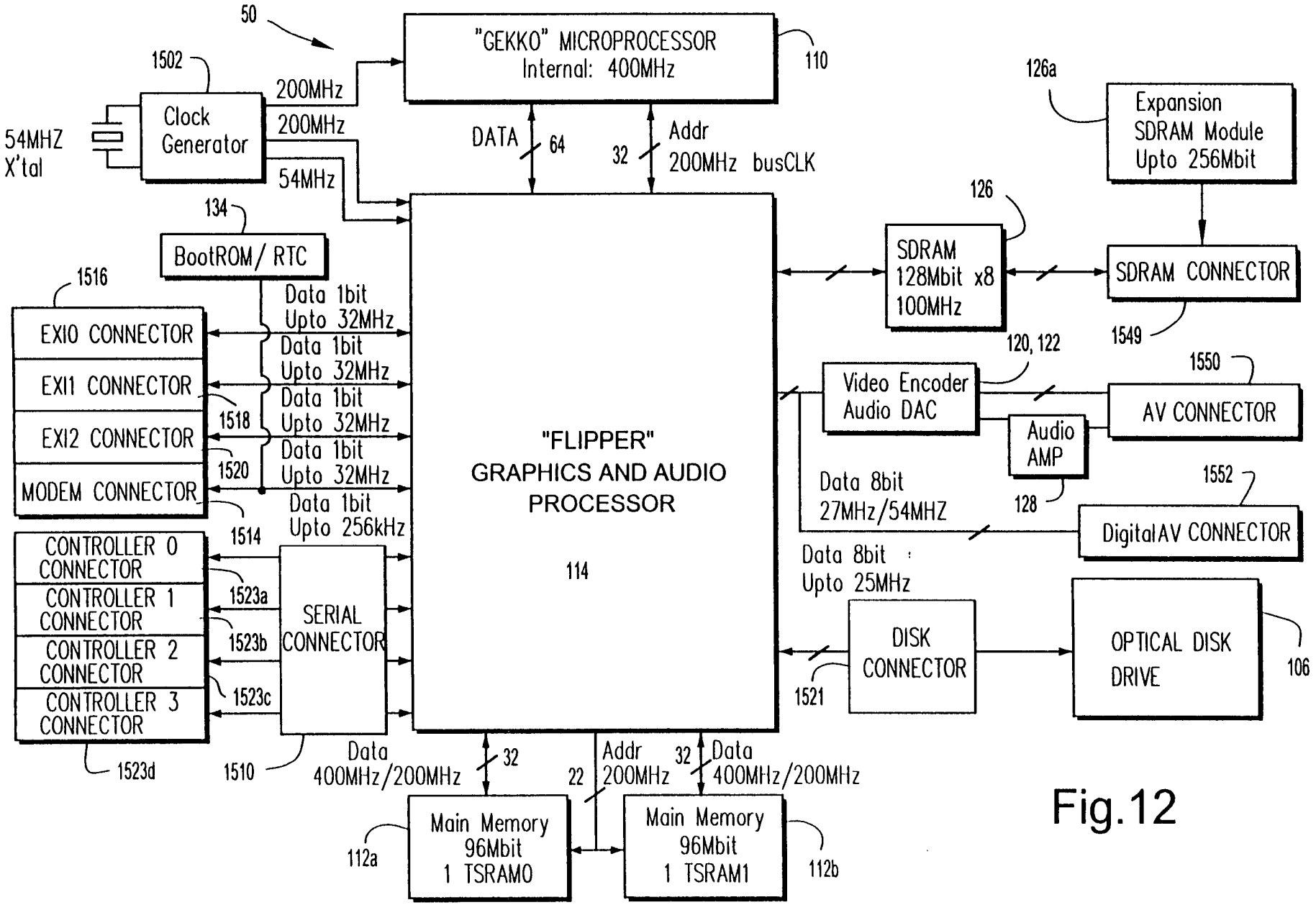

50
"GEKKO" MICROPROCESSOR
Internal: 400MHz
110
1502
Clock
Generator
200MHz
200MHz
54MHz
54MHZ
X'tal
DATA
64
32
Addr
200MHz busCLK
126a
Expansion
SDRAM Module
Upto 256Mbit
126
SDRAM
128Mbit x8
100MHz
SDRAM CONNECTOR
1549
134
BootROM/ RTC
1516
EXI0 CONNECTOR
EXI1 CONNECTOR
EXI2 CONNECTOR
MODEM CONNECTOR
1518
1520
Data 1bit
Upto 32MHz
Data 1bit
Upto 32MHz
Data 1bit
Upto 32MHz
Data 1bit
Upto 32MHz
Data 1bit
Upto 256kHz
"FLIPPER"
GRAPHICS AND AUDIO
PROCESSOR
114
120, 122
Video Encoder
Audio DAC
1550
AV CONNECTOR
Audio
AMP
128
Data 8bit
27MHz/54MHZ
1552
DigitalAV CONNECTOR
Data 8bit
Upto 25MHz
1514
CONTROLLER 0
CONNECTOR
CONTROLLER 1
CONNECTOR
CONTROLLER 2
CONNECTOR
CONTROLLER 3
CONNECTOR
1523a
1523b
1523c
1523d
SERIAL
CONNECTOR
1510
DISK
CONNECTOR
1521
OPTICAL DISK
DRIVE
106
Data
400MHz/200MHz
32
Addr
200MHz
22
32
Data
400MHz/200MHz
Main Memory
96Mbit
1 TSRAM0
112a
Main Memory
96Mbit
1 TSRAM1
112b

Fig.12

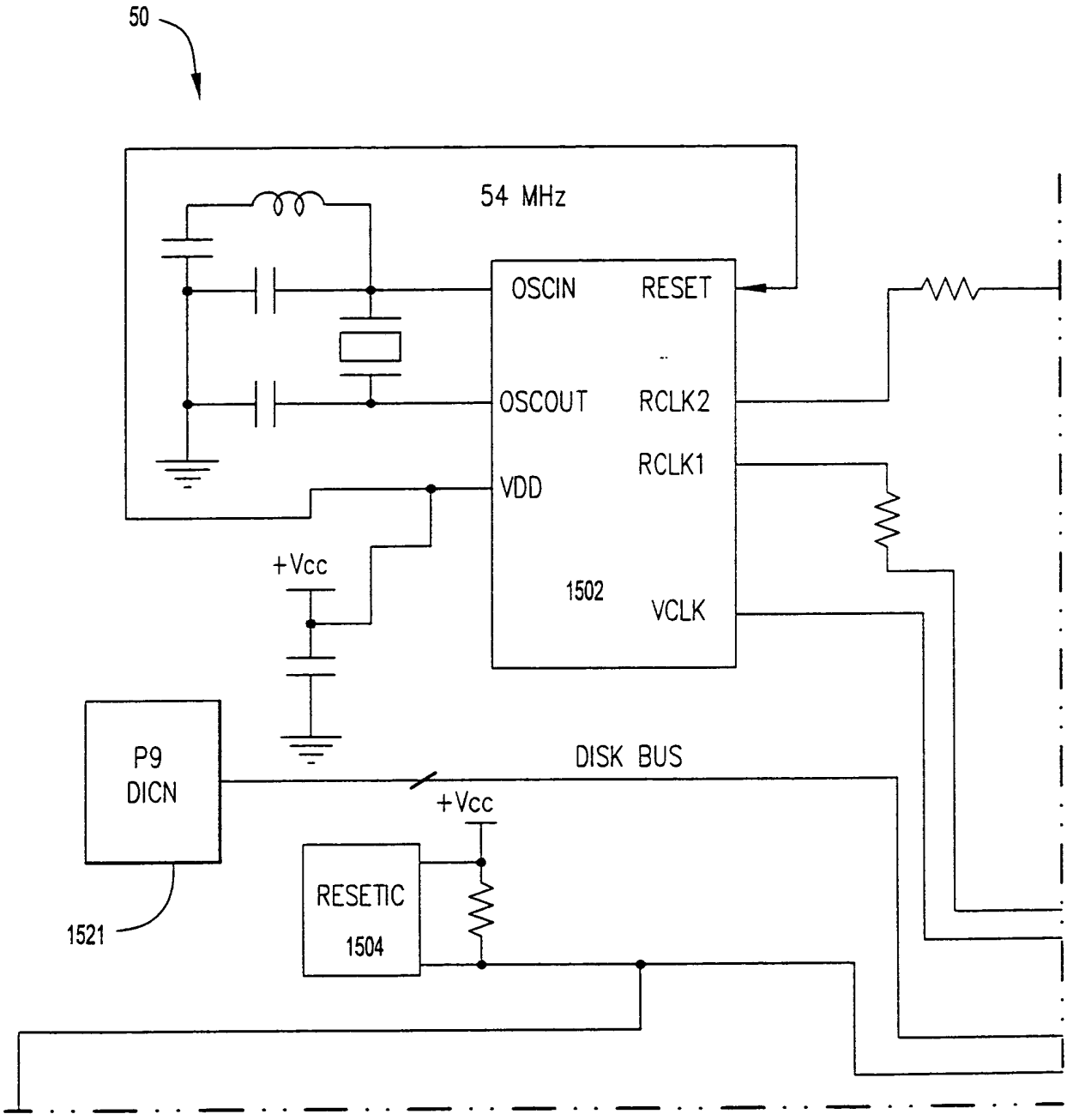
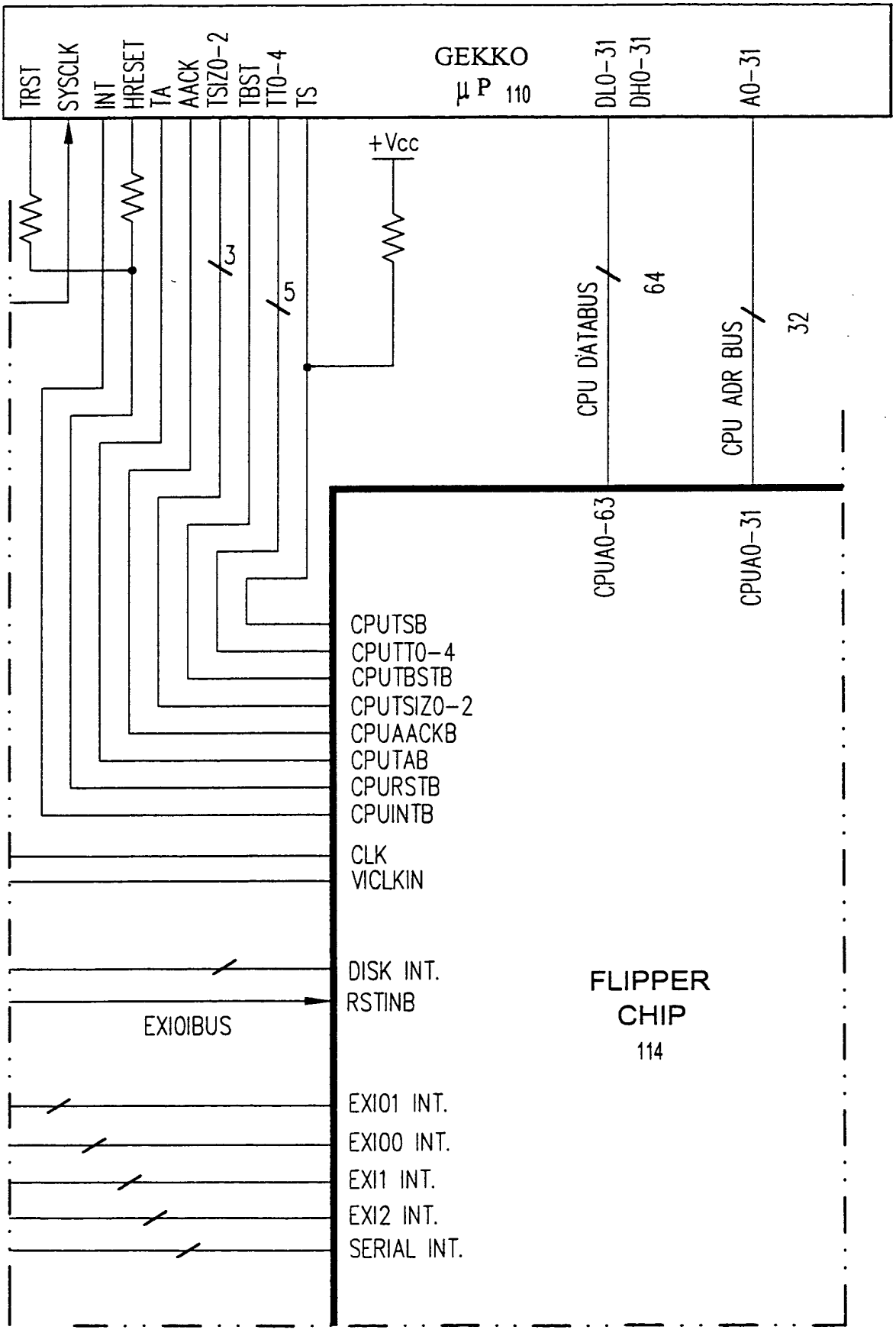

50
54 MHz
OSCIN
RESET
OSCOUT
RCLK2
RCLK1
VDD
+Vcc
1502
VCLK
P9
DICN
DISK BUS
+Vcc
RESETIC
1504
1521

Fig.12A

Fig.12B


TRST
SYSCLK
INT
HRESET
TA
AACK
TSIZ0-2
TBST
TT0-4
TS
GEKKO
μP 110
DL0-31
DH0-31
A0-31
+Vcc
3
5
CPU DATABUS
64
CPU ADR BUS
32
CPUA0-63
CPUA0-31
CPUTSB
CPUTT0-4
CPUTBSTB
CPUTSIZ0-2
CPUAACKB
CPUTAB
CPURSTB
CPUINTB
CLK
VICLKIN
DISK INT.
RSTINB
EXI0IBUS
FLIPPER
CHIP
114
EXI01 INT.
EXI00 INT.
EXI1 INT.
EXI2 INT.
SERIAL INT.

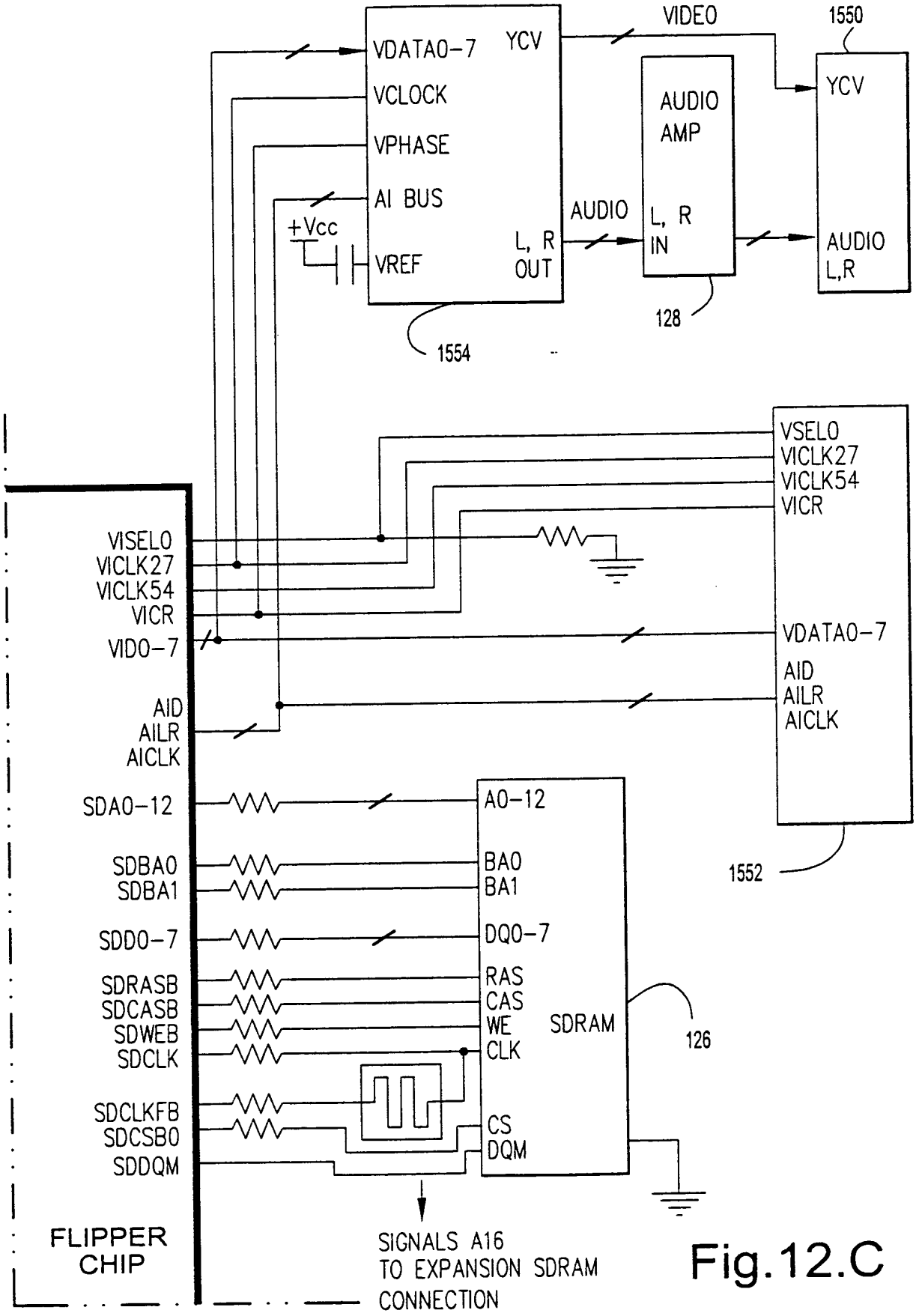
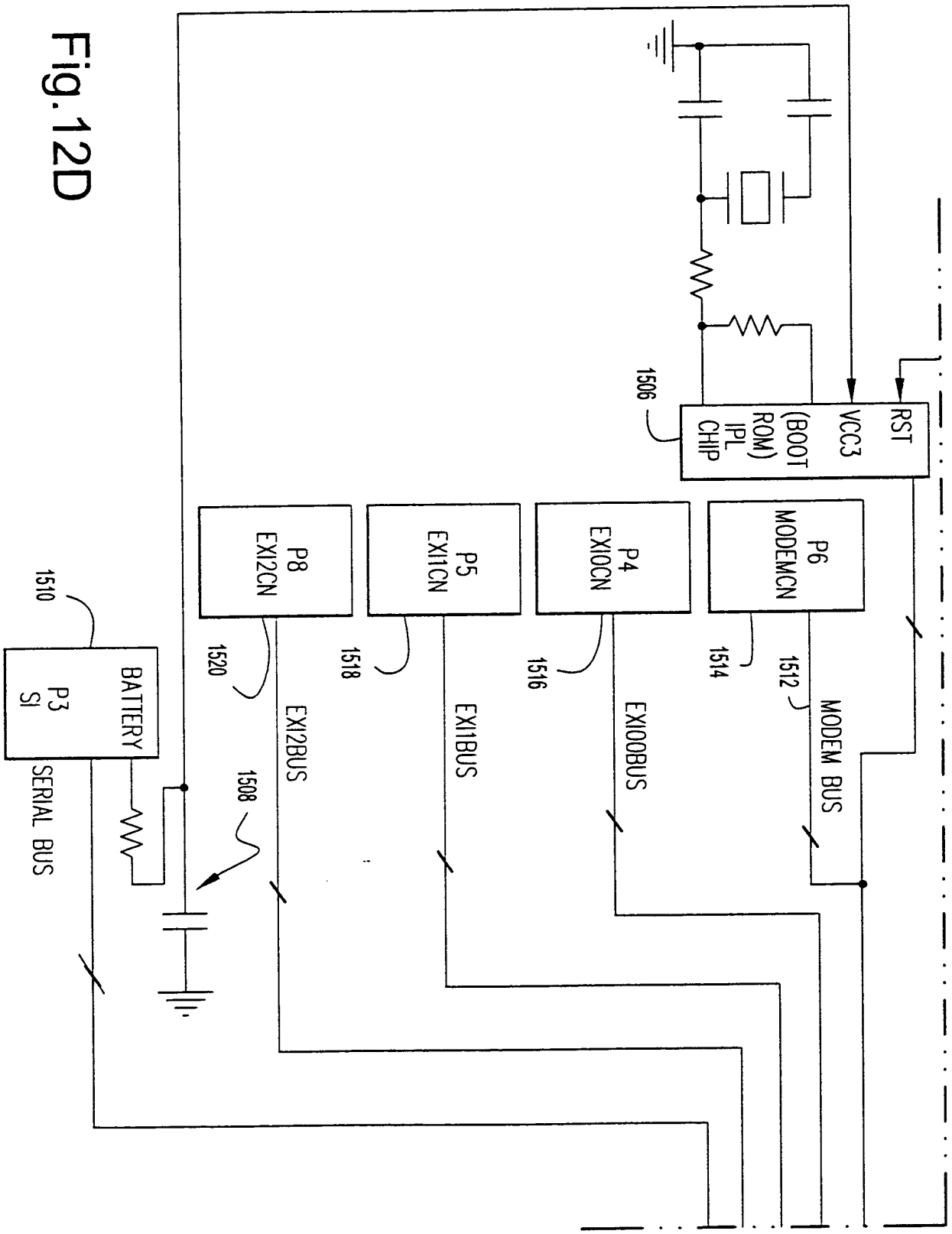

VDATA0-7
YCV
VCLOCK
VPHASE
AI BUS
+Vcc
VREF
L, R
OUT
AUDIO
VIDEO
1550
YCV
AUDIO
AMP
L, R
IN
AUDIO
L,R
128
1554
VSEL0
VICLK27
VICLK54
VICR
VDATA0-7
AID
AILR
AICLK
1552
VISEL0
VICLK27
VICLK54
VICR
VID0-7
AID
AILR
AICLK
SDA0-12
SDBA0
SDBA1
SDD0-7
SDRASB
SDCASB
SDWEB
SDCLK
SDCLKFB
SDCSB0
SDDQM
A0-12
BA0
BA1
DQ0-7
RAS
CAS
WE
CLK
CS
DQM
SDRAM
126
FLIPPER
CHIP
SIGNALS A16
TO EXPANSION SDRAM
CONNECTION

Fig.12.C

Fig.12D


1506
IPL CHIP (BOOT ROM)
VCC3
RST
P6 MODEMCN
P4 EXI0CN
P5 EXI1CN
P8 EXI2CN
1514
1512
1516
1518
1520
MODEM BUS
EXI0BUS
EXI1BUS
EXI2BUS
1508
1510
P3 SI
BATTERY
SERIAL BUS

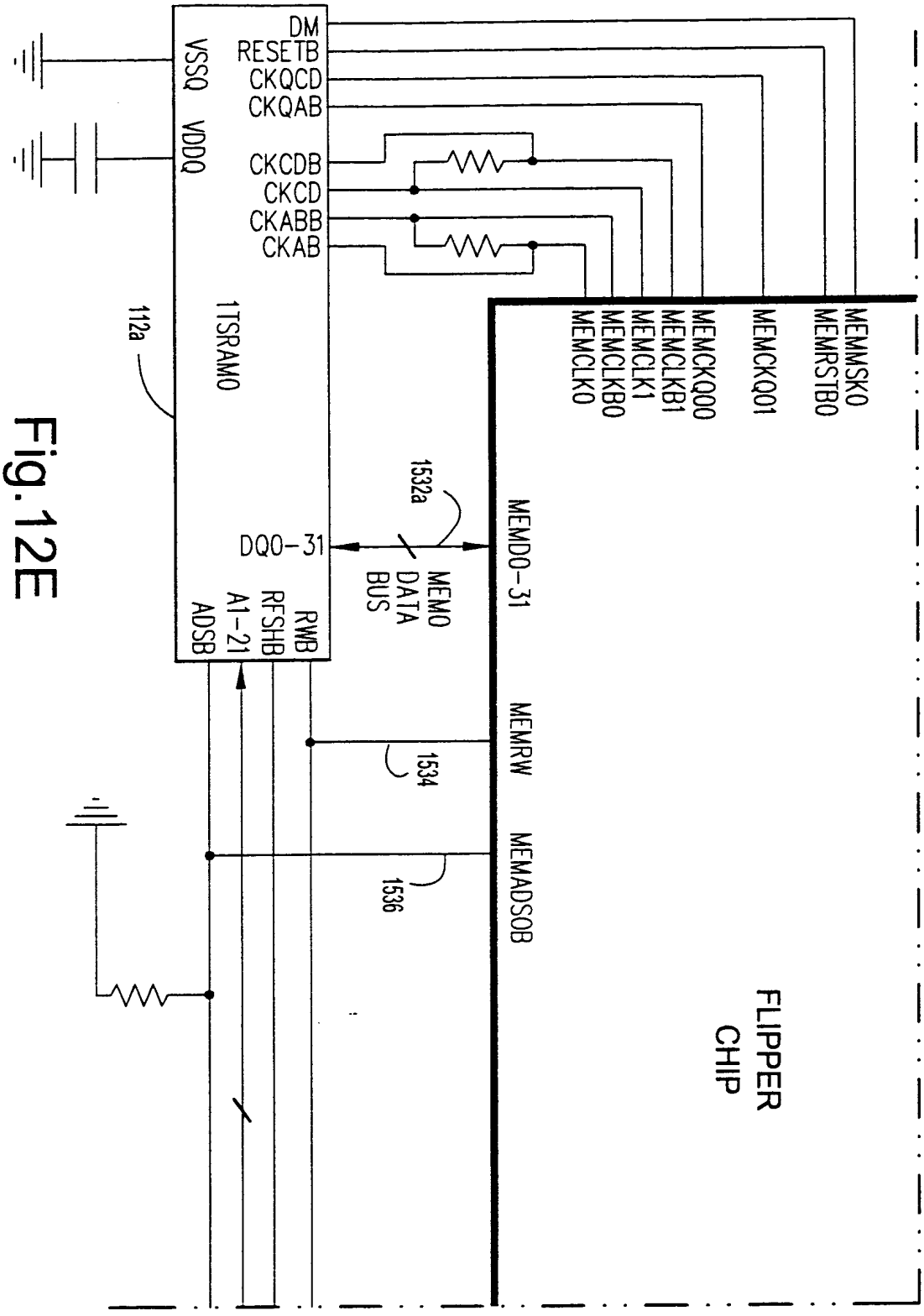

DM
RESETB
CKQCD
CKQAB
CKCDB
CKCD
CKABB
CKAB
VSSQ
VDDQ
112a
1TSRAM0
DQ0-31
RWB
RFSHB
A1-21
ADSB
1532a
MEMO DATA BUS
MEMD0-31
MEMRW
MEMADSOB
1534
1536
MEMMSK0
MEMRSTB0
MEMCKQ01
MEMCKQ00
MEMCLKB1
MEMCLK1
MEMCLKB0
MEMCLK0
FLIPPER CHIP

Fig.12E

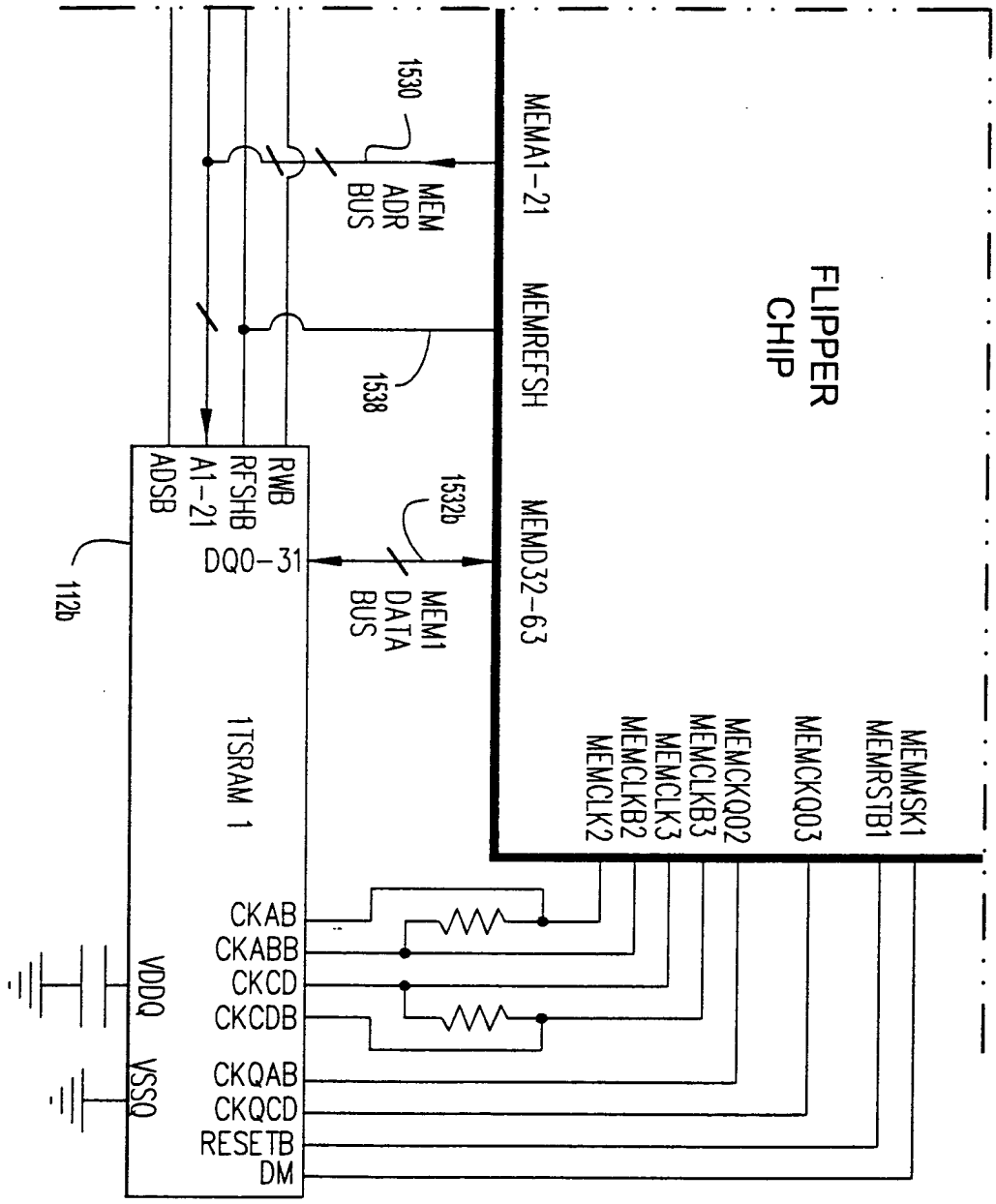

FLIPPER CHIP
MEMA1-21
MEMREFSH
MEMD32-63
MEMCKQ03
MEMCKQ02
MEMCLK3
MEMCLKB3
MEMCLKB2
MEMCLK2
MEMMSK1
MEMRSTB1
1530
MEM ADR BUS
1538
1532b
MEM1 DATA BUS
112b
ADSB
A1-21
RFSHB
RWB
DQ0-31
1TSRAM 1
CKAB
CKABB
CKCD
CKCDB
CKQAB
CKQCD
RESETB
DM
VDDQ
VSSQ

Fig.12F

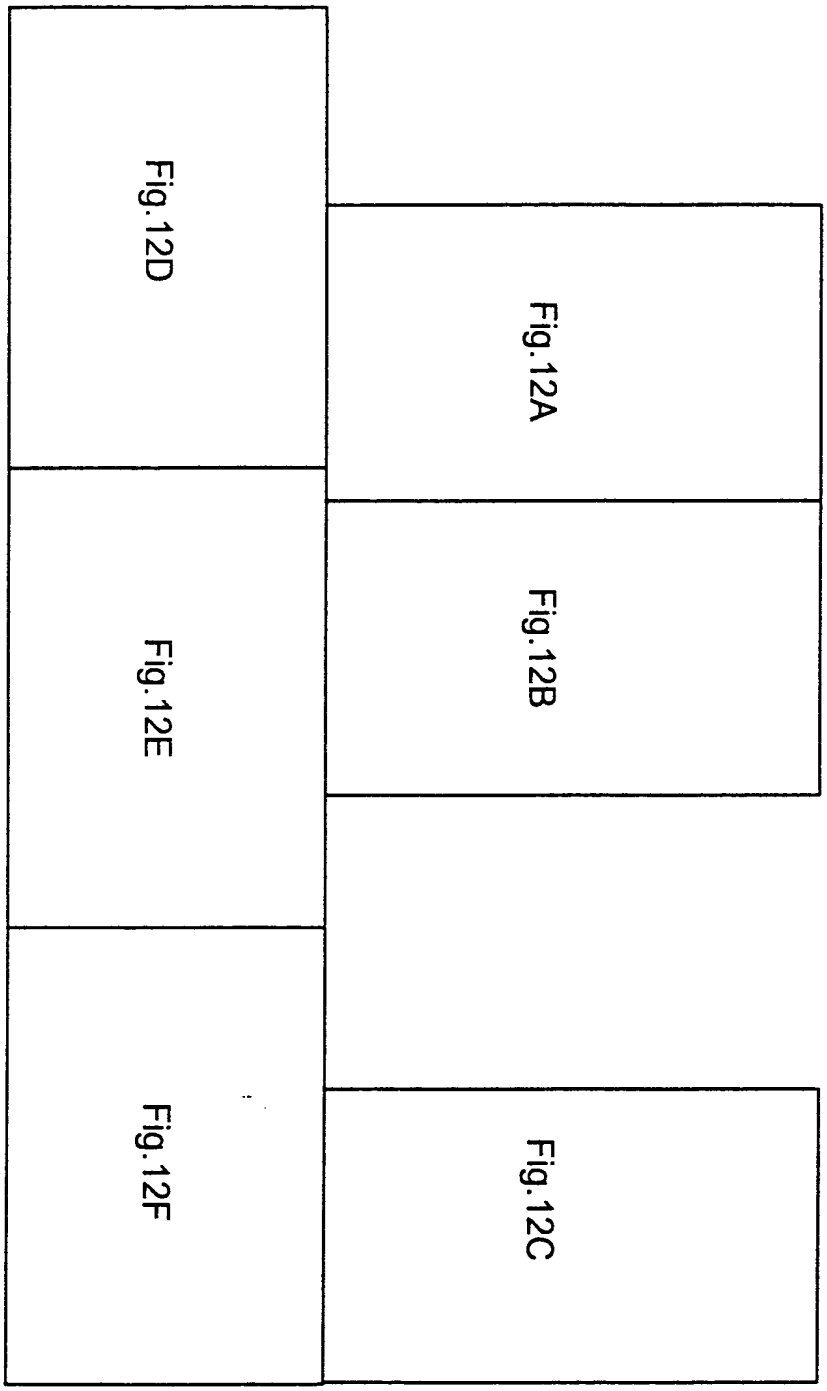



Fig.12G

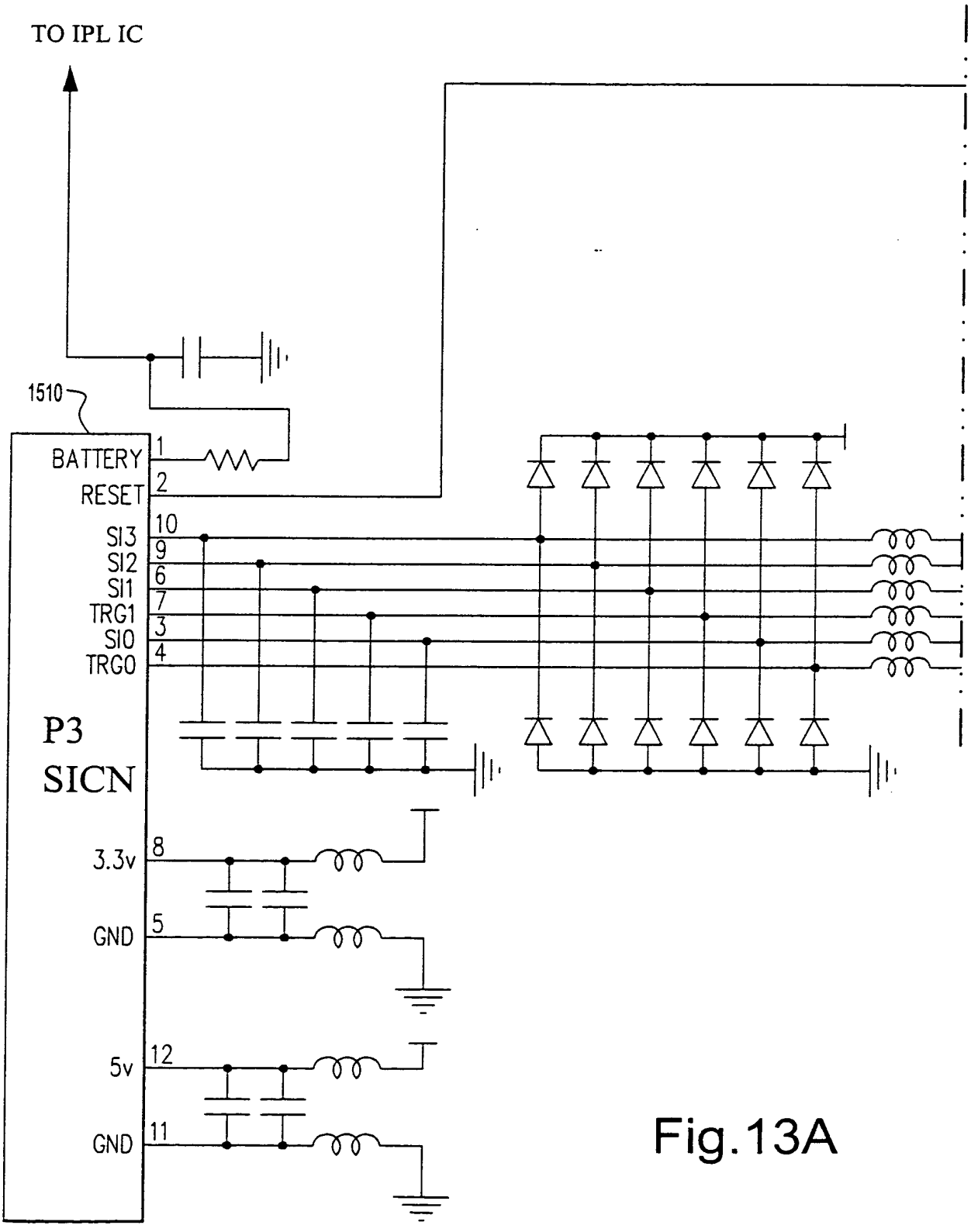

TO IPL IC
1510
BATTERY
RESET
SI3
SI2
SI1
TRG1
SI0
TRG0
P3
SICN
3.3v
GND
5v
GND
1
2
10
9
6
7
3
4
8
5
12
11

Fig.13A

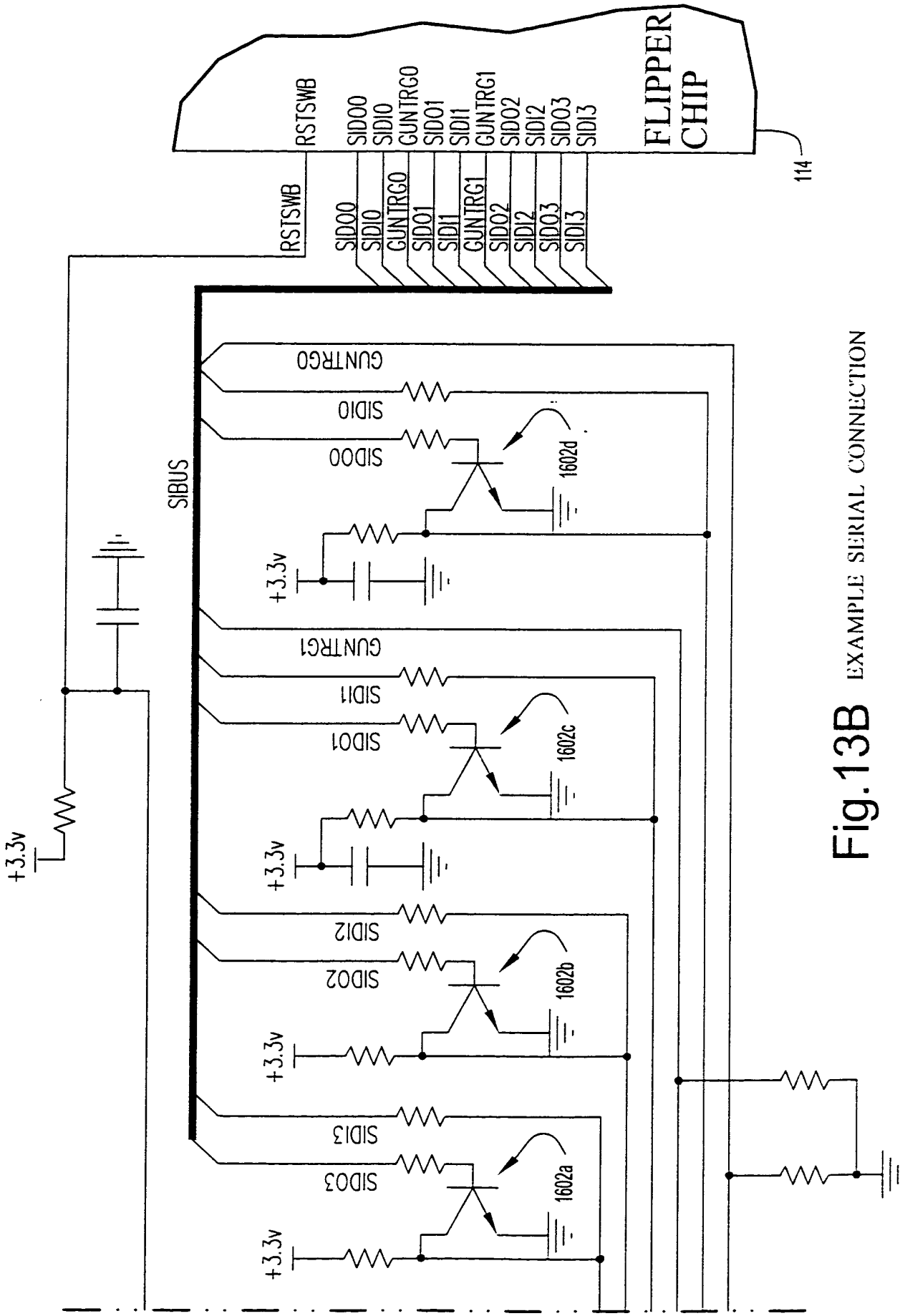



Fig.13B EXAMPLE SERIAL CONNECTION

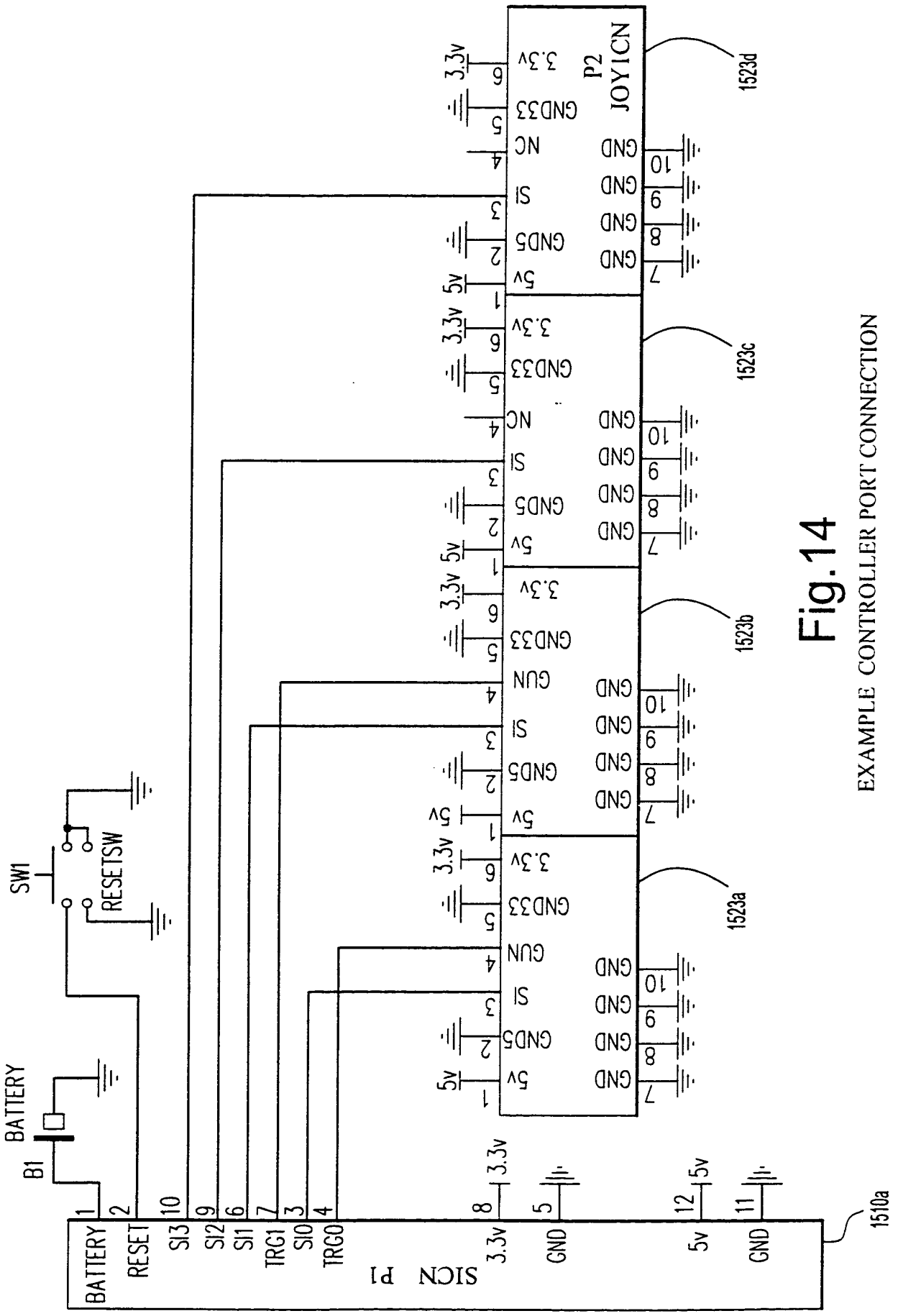



Fig.14

EXAMPLE CONTROLLER PORT CONNECTION

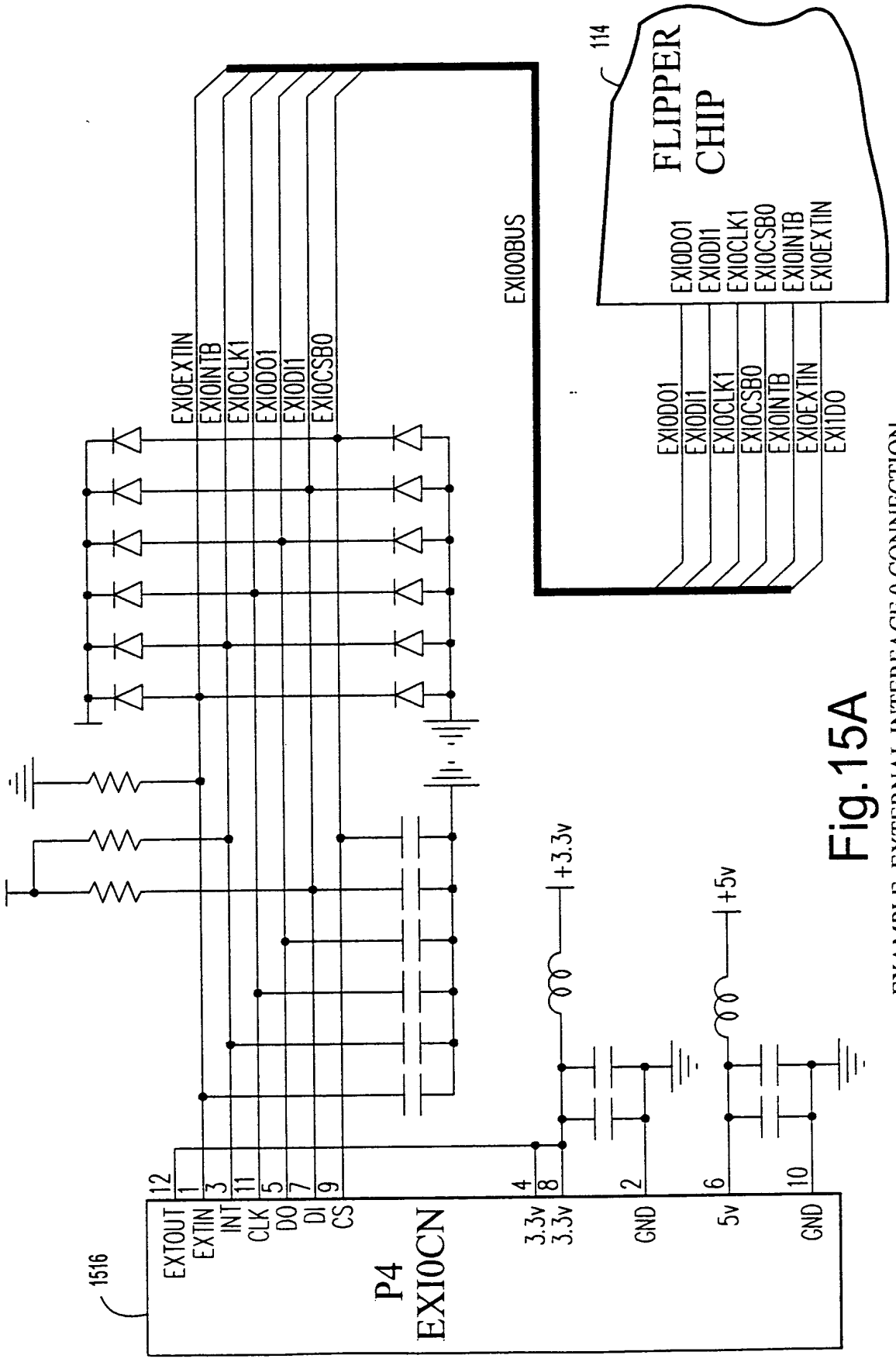



Fig.15A

EXAMPLE EXTERNAL INTERFACE 0 CONNECTION

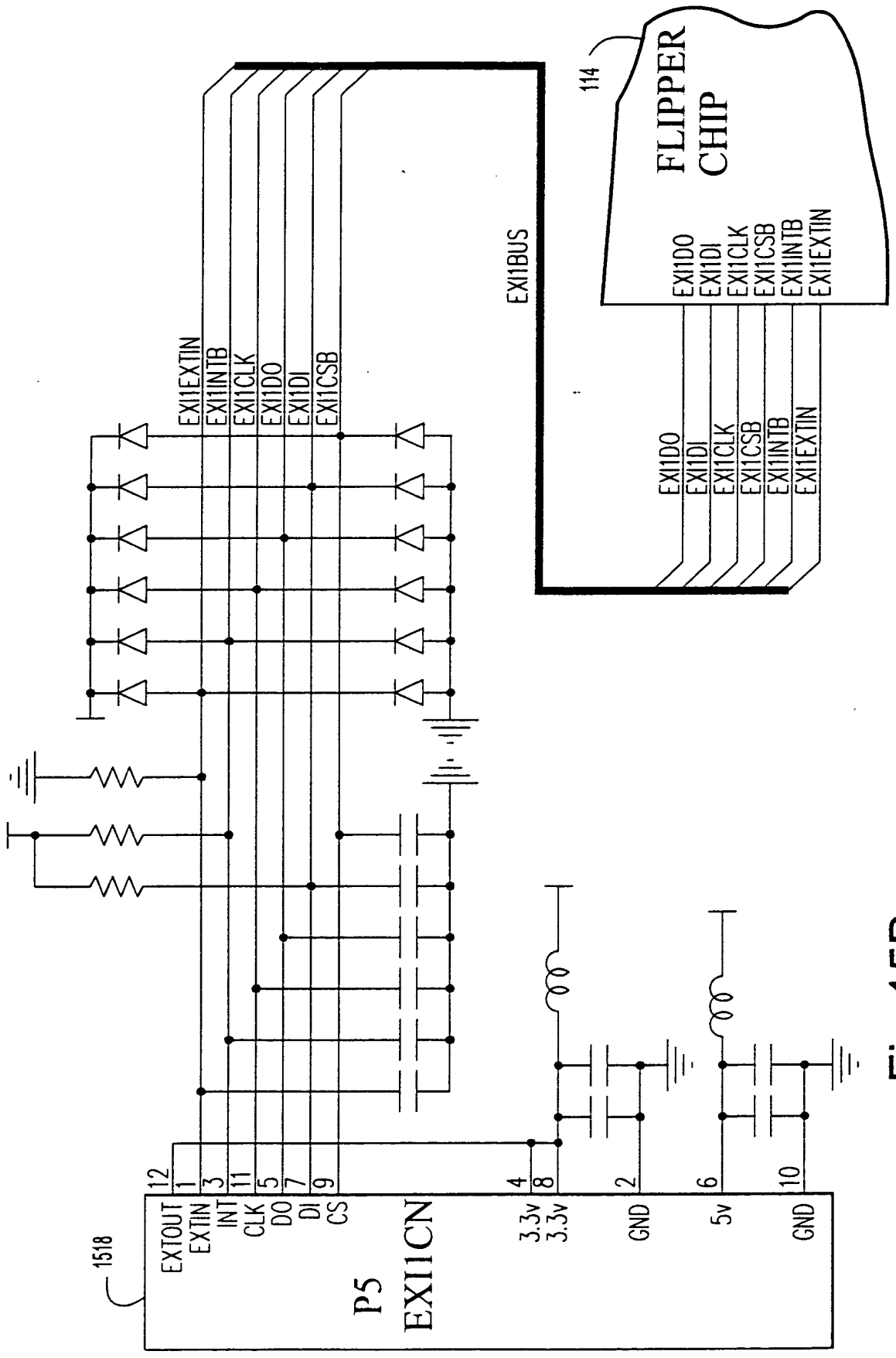



Fig.15B EXAMPLE EXTERNAL INTERFACE 1 CONNECTION

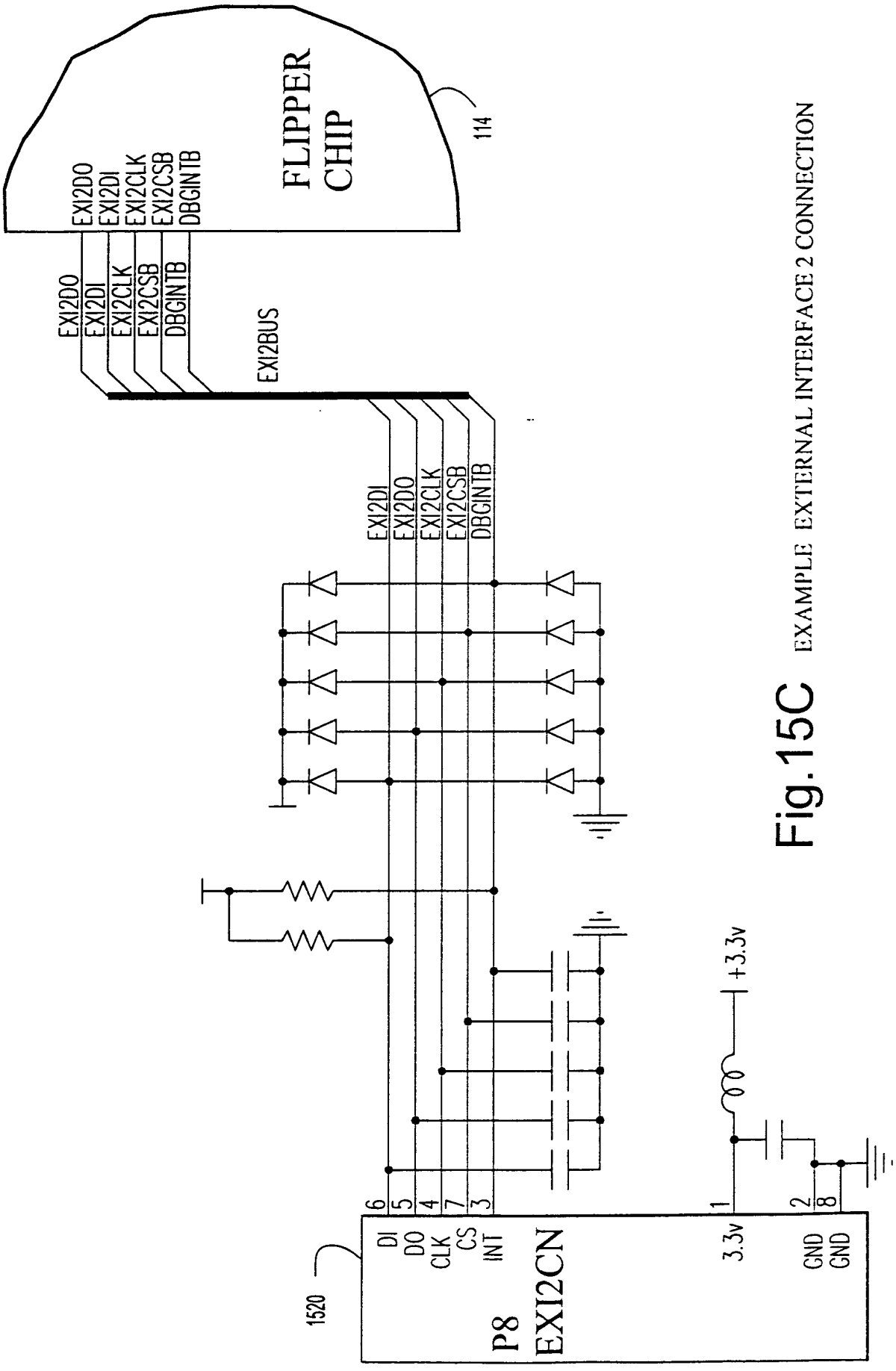



Fig.15C EXAMPLE EXTERNAL INTERFACE 2 CONNECTION

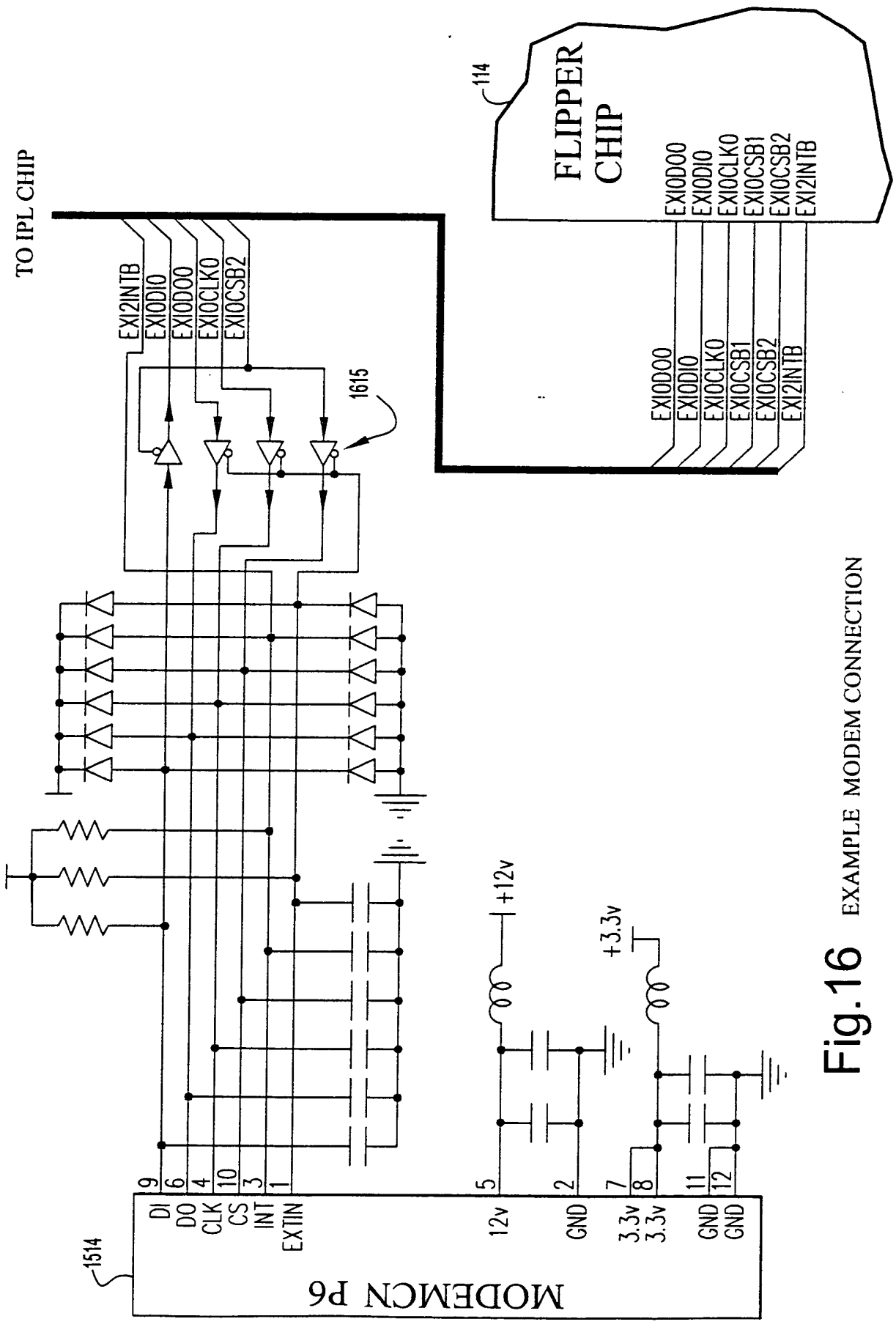



Fig.16 EXAMPLE MODEM CONNECTION

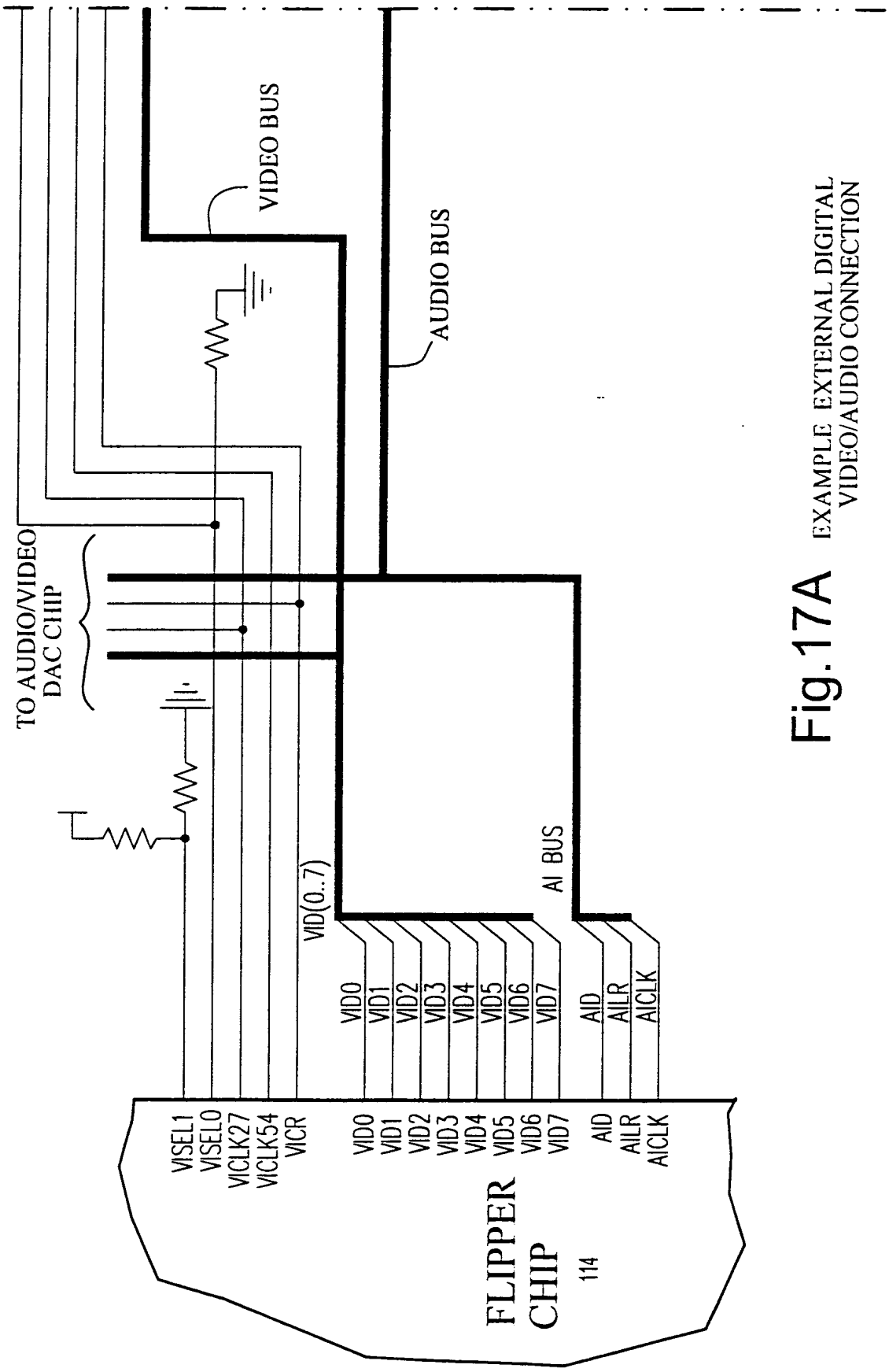



Fig.17A EXAMPLE EXTERNAL DIGITAL VIDEO/AUDIO CONNECTION

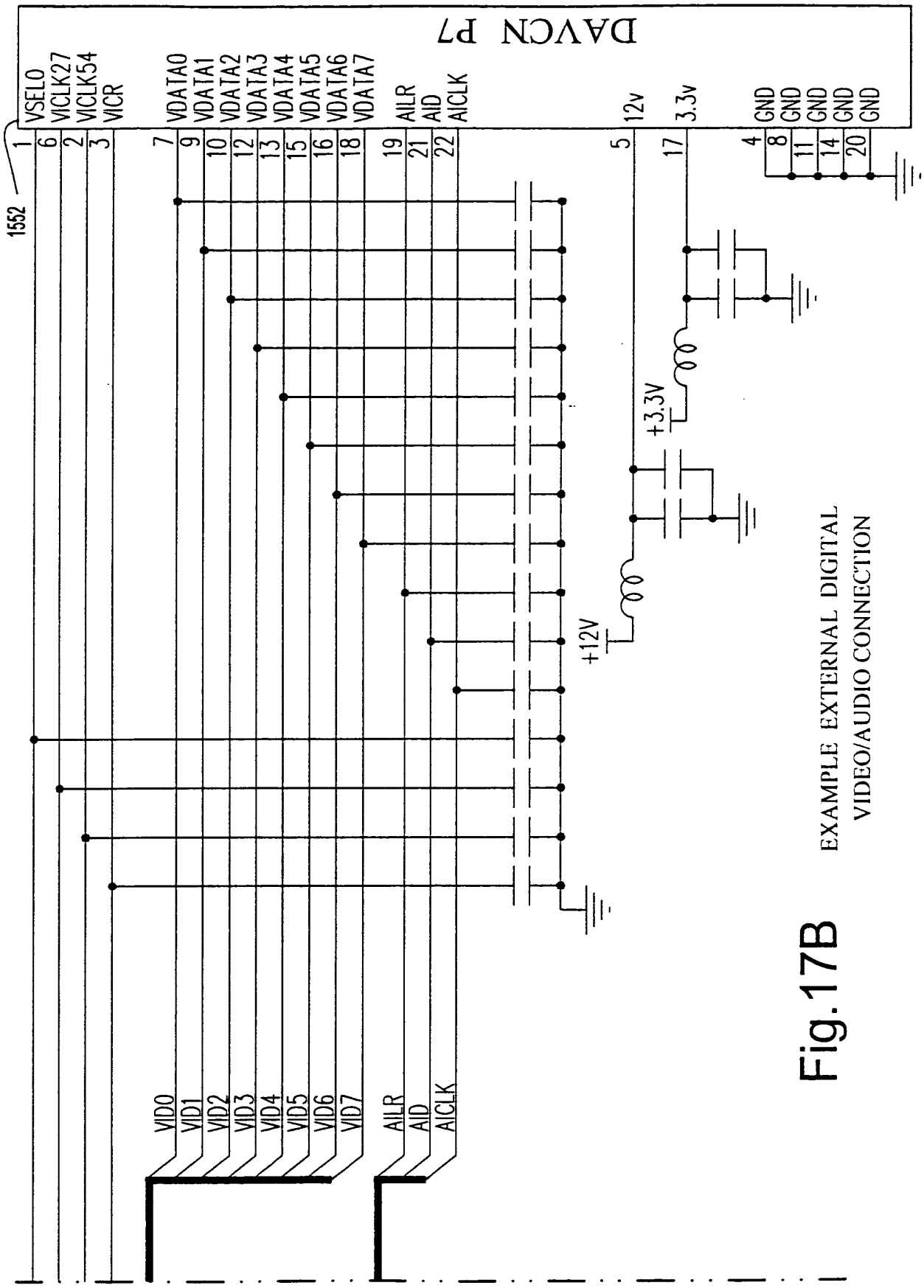



Fig.17B EXAMPLE EXTERNAL DIGITAL VIDEO/AUDIO CONNECTION

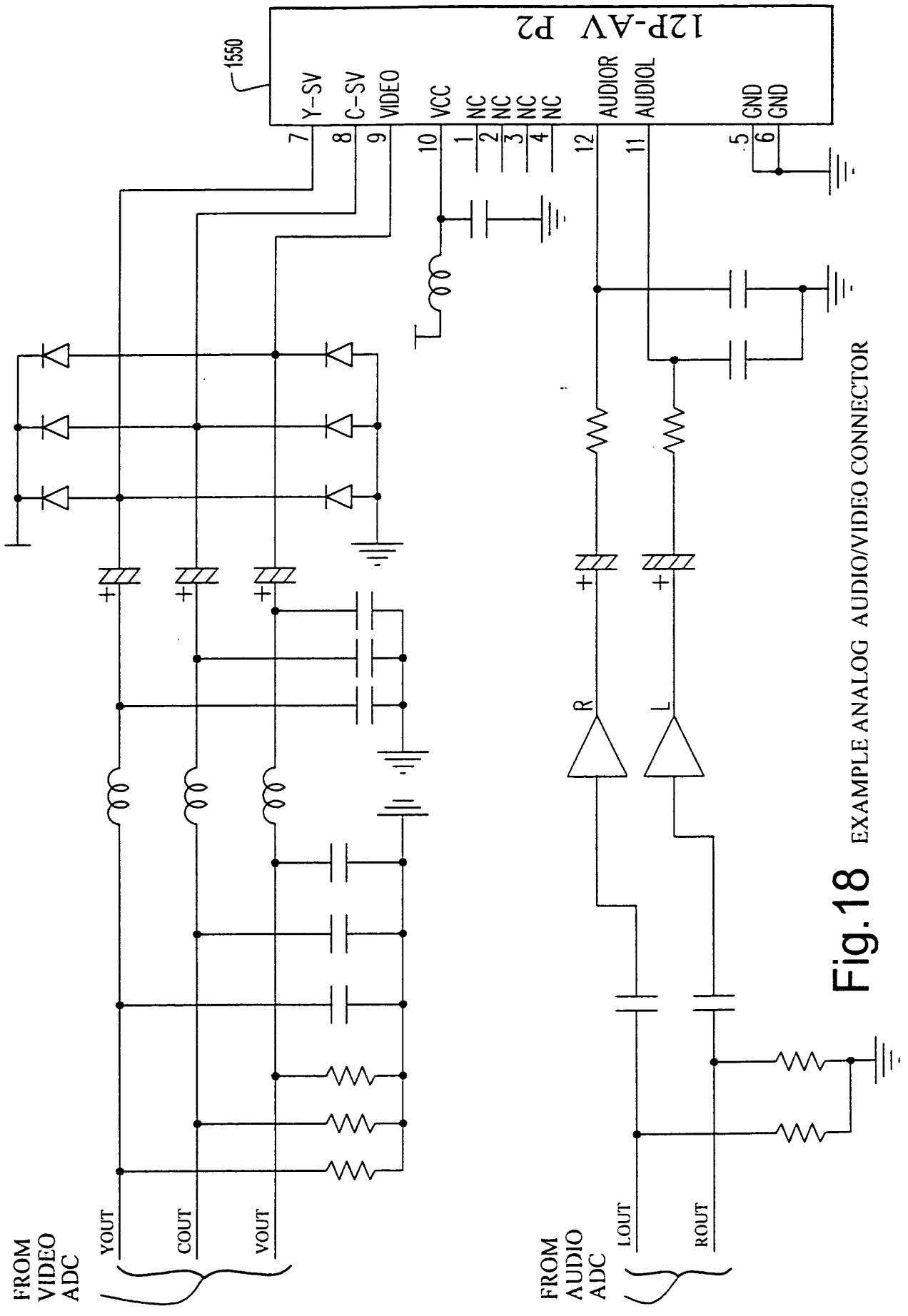



Fig.18 EXAMPLE ANALOG AUDIO/VIDEO CONNECTOR

Fig.19A

EXAMPLE SDRAM EXPANSION CONNECTION

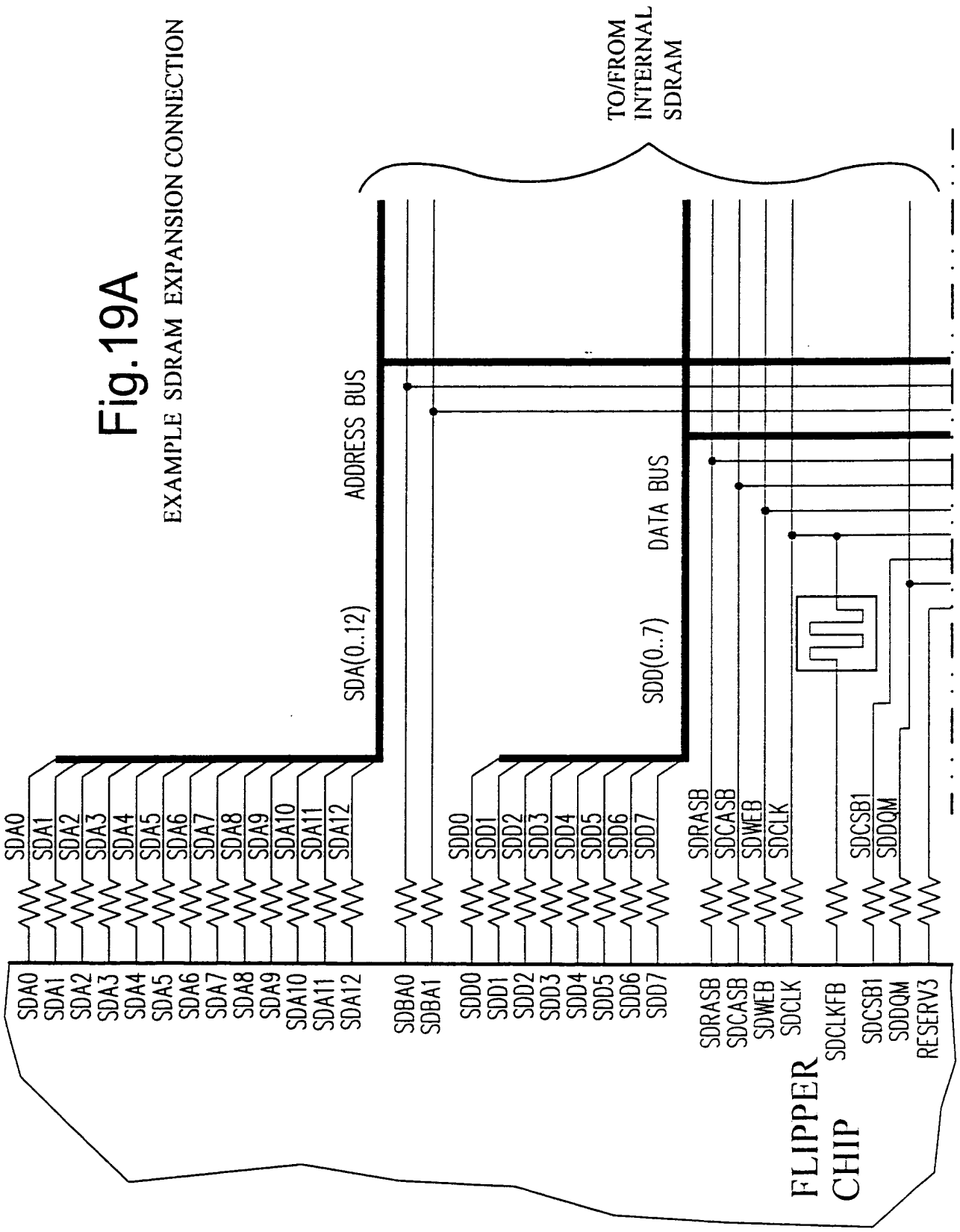
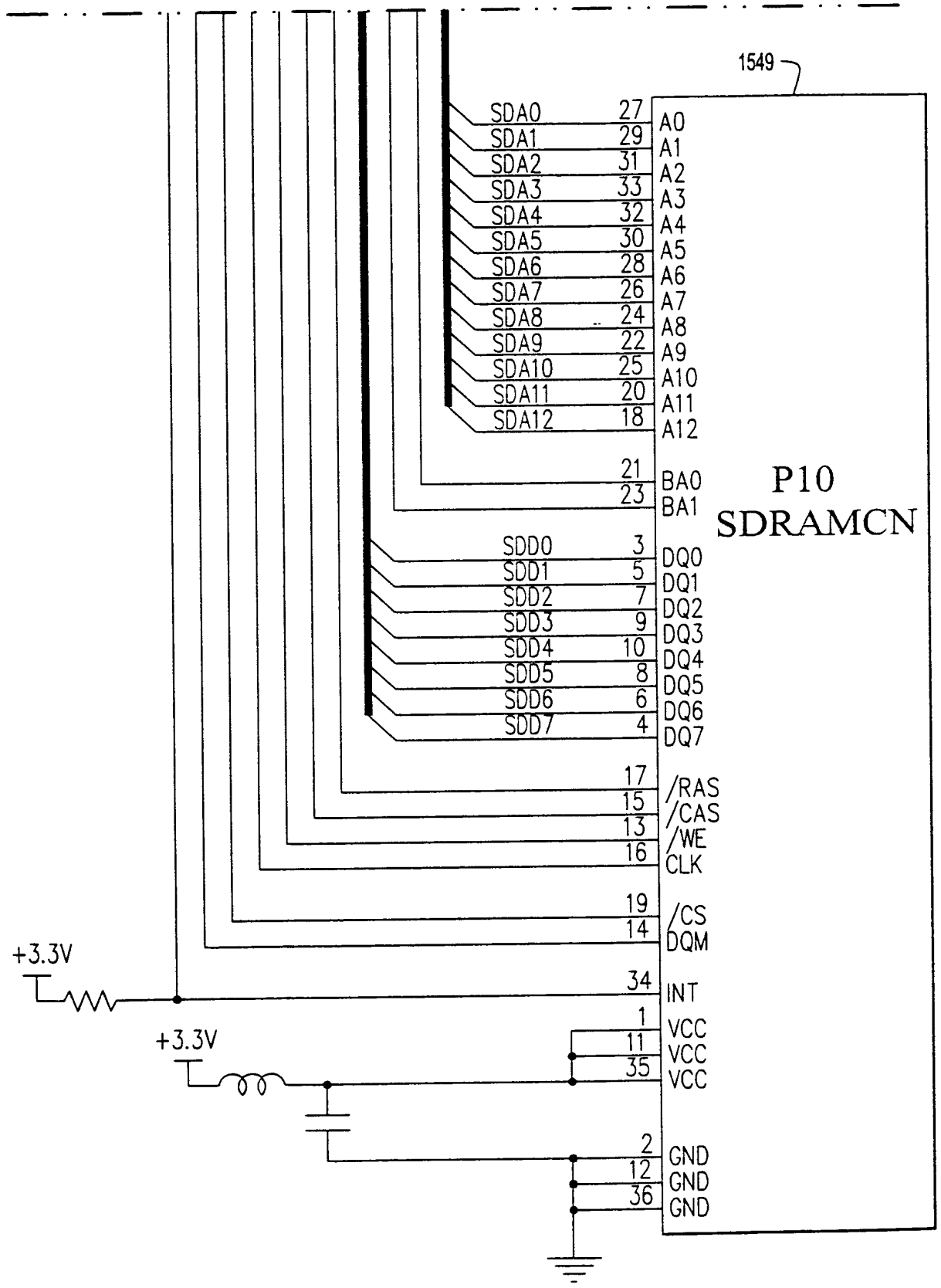


Fig.19B


1549
SDA0
SDA1
SDA2
SDA3
SDA4
SDA5
SDA6
SDA7
SDA8
SDA9
SDA10
SDA11
SDA12
27
29
31
33
32
30
28
26
24
22
25
20
18
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
21
23
BA0
BA1
P10
SDRAMCN
SDD0
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
3
5
7
9
10
8
6
4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
17
15
13
16
/RAS
/CAS
/WE
CLK
19
14
/CS
DQM
+3.3V
34
INT
+3.3V
1
11
35
VCC
VCC
VCC
2
12
36
GND
GND
GND

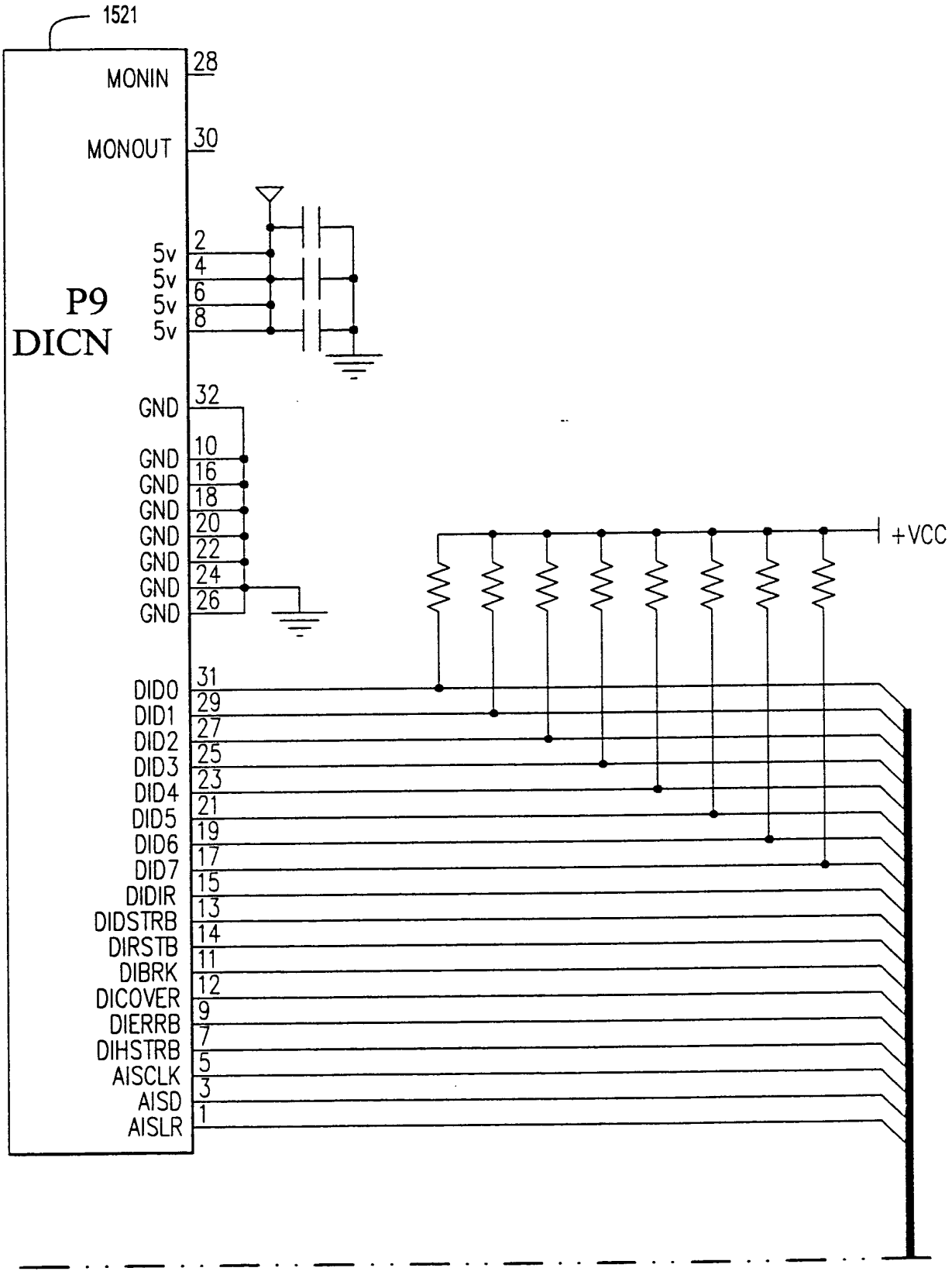



Fig.20A EXAMPLE DISK DRIVE CONNECTION

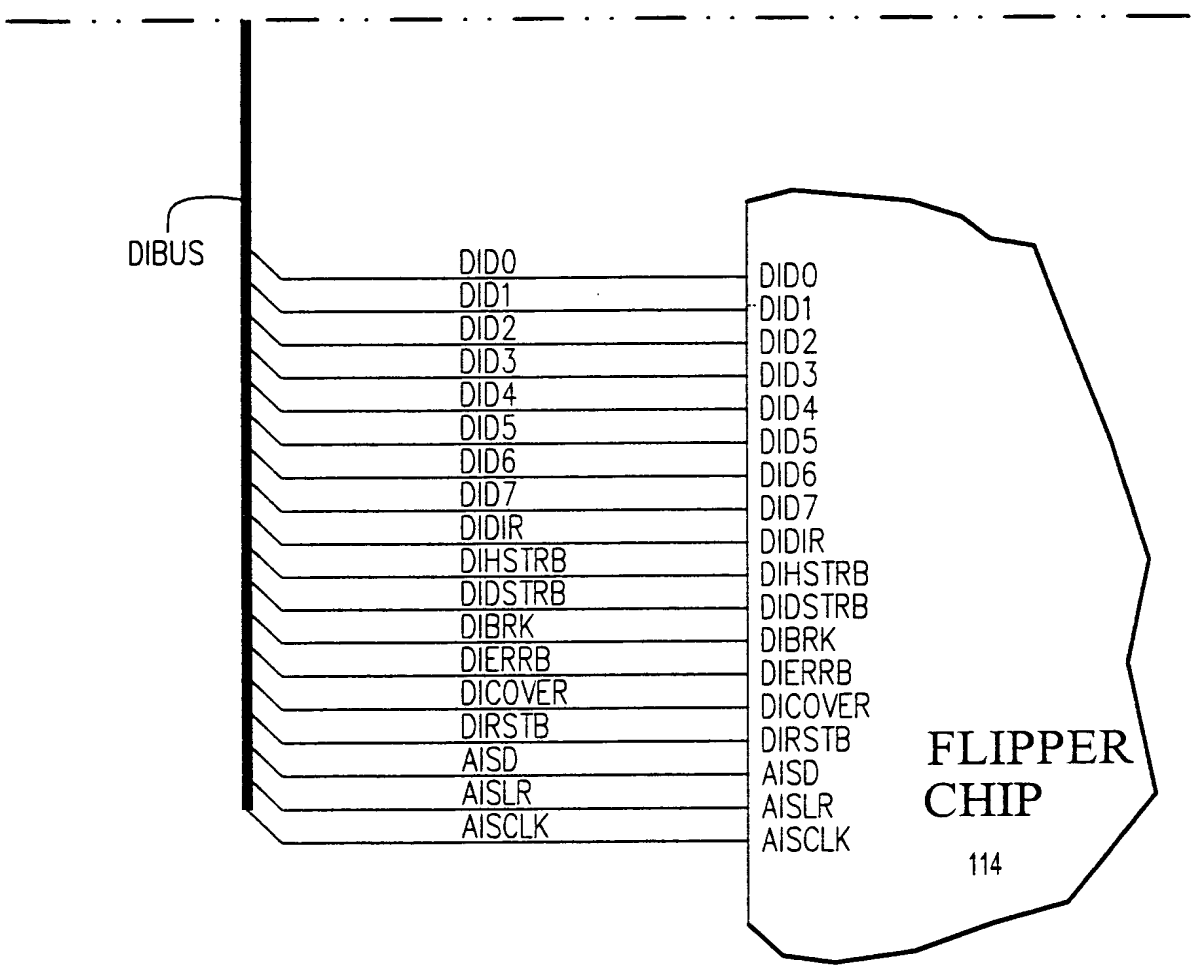



Fig.20B

EXAMPLE DISK DRIVE CONNECTION

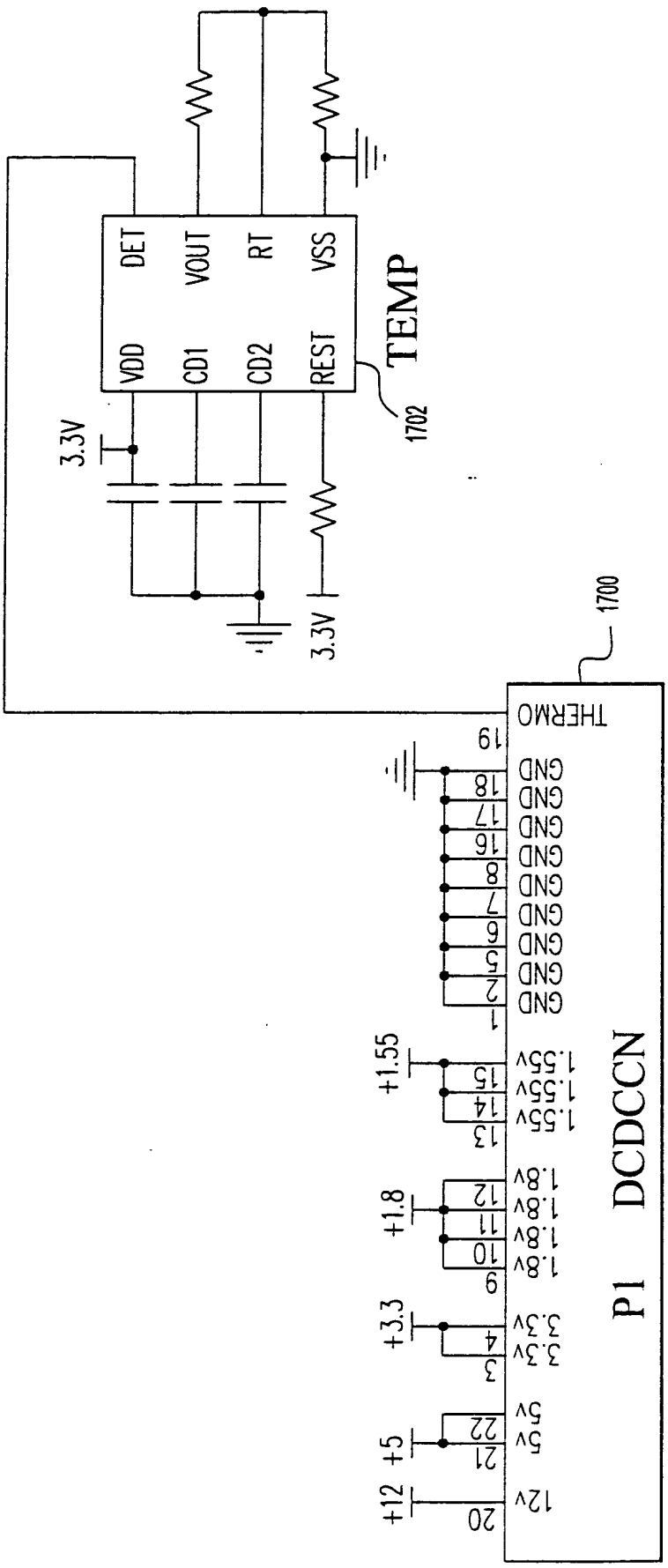



Fig.21 EXAMPLE POWER SUPPLY CONNECTION

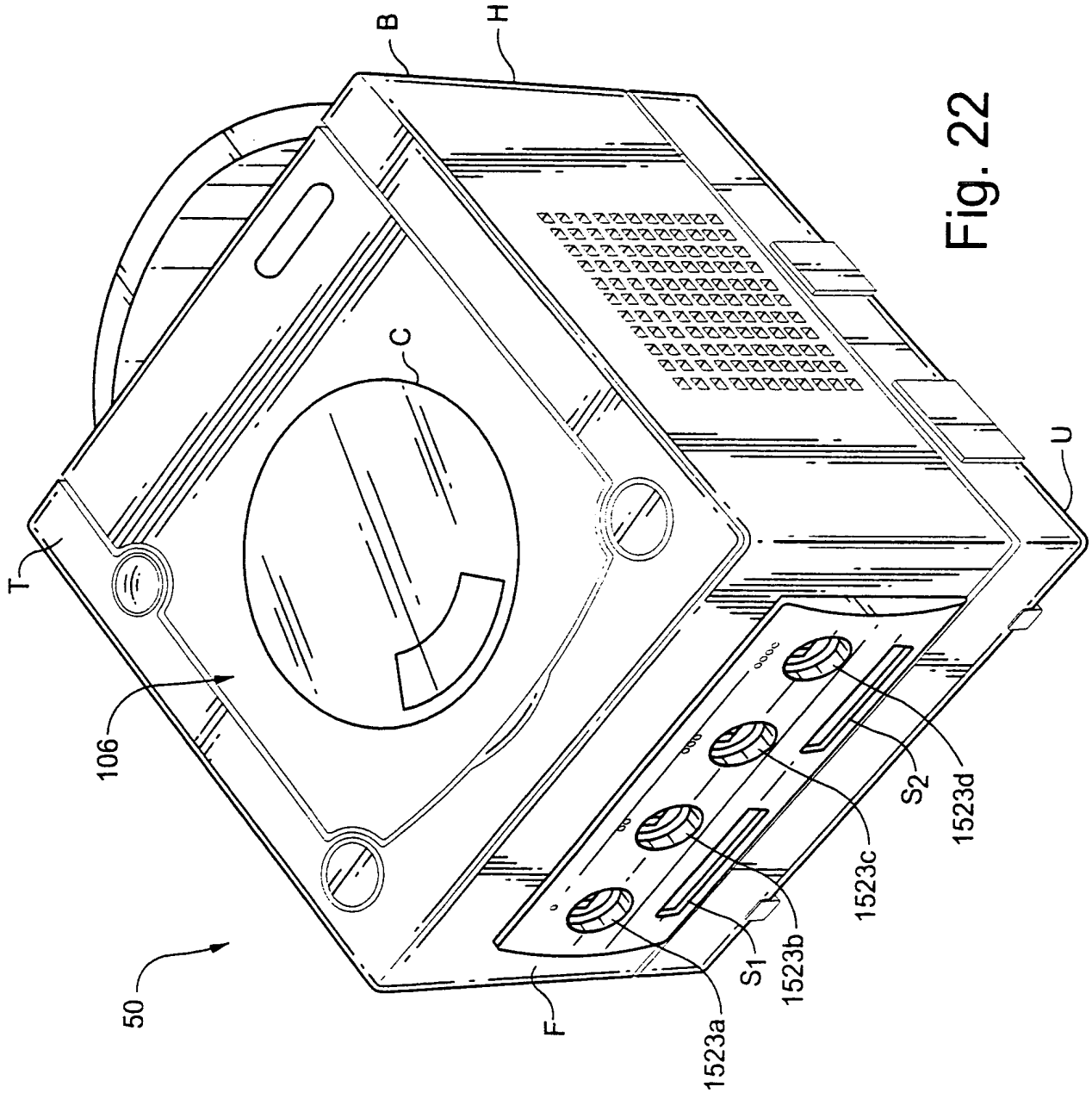



Fig. 22

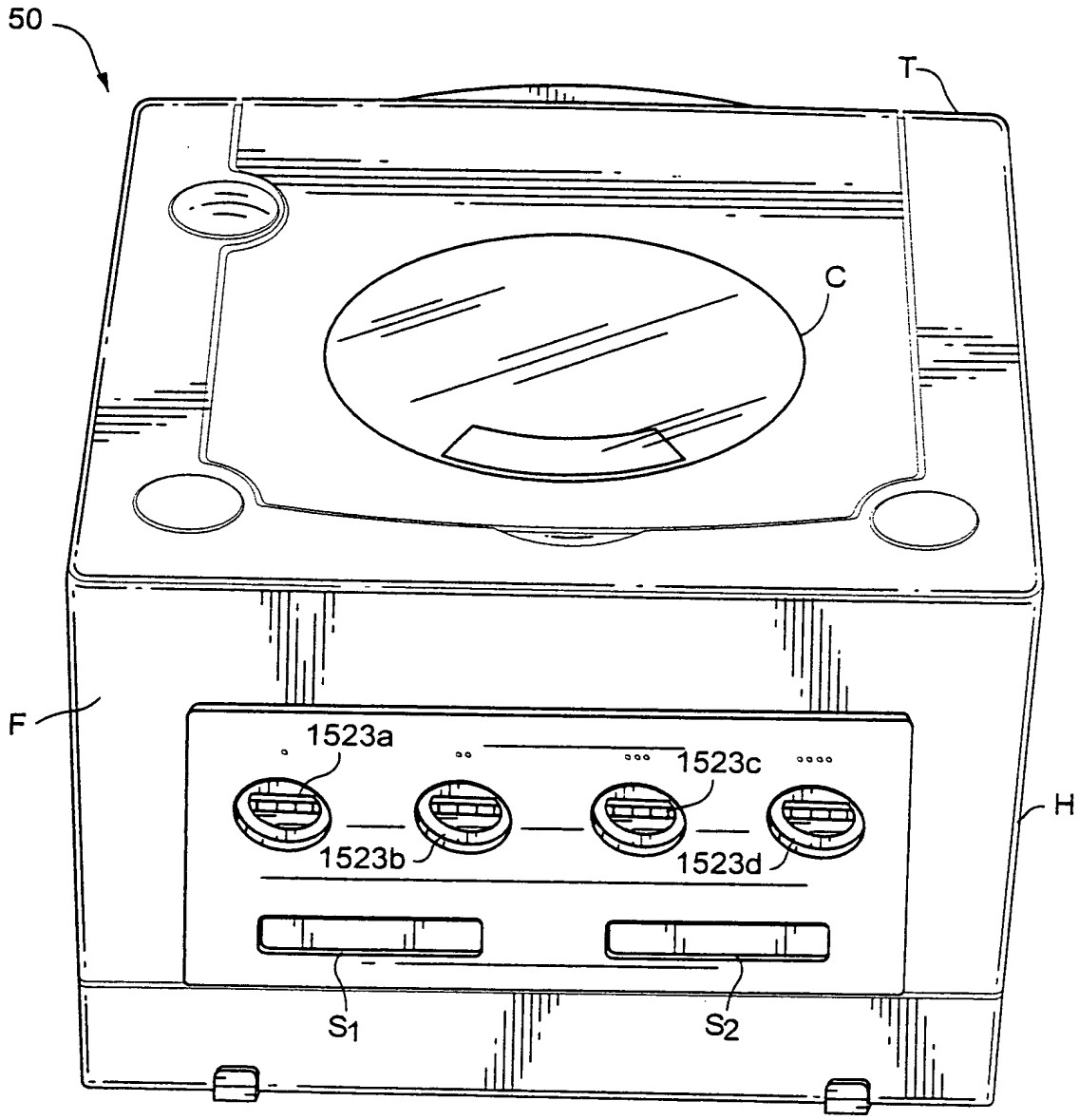



Fig. 23

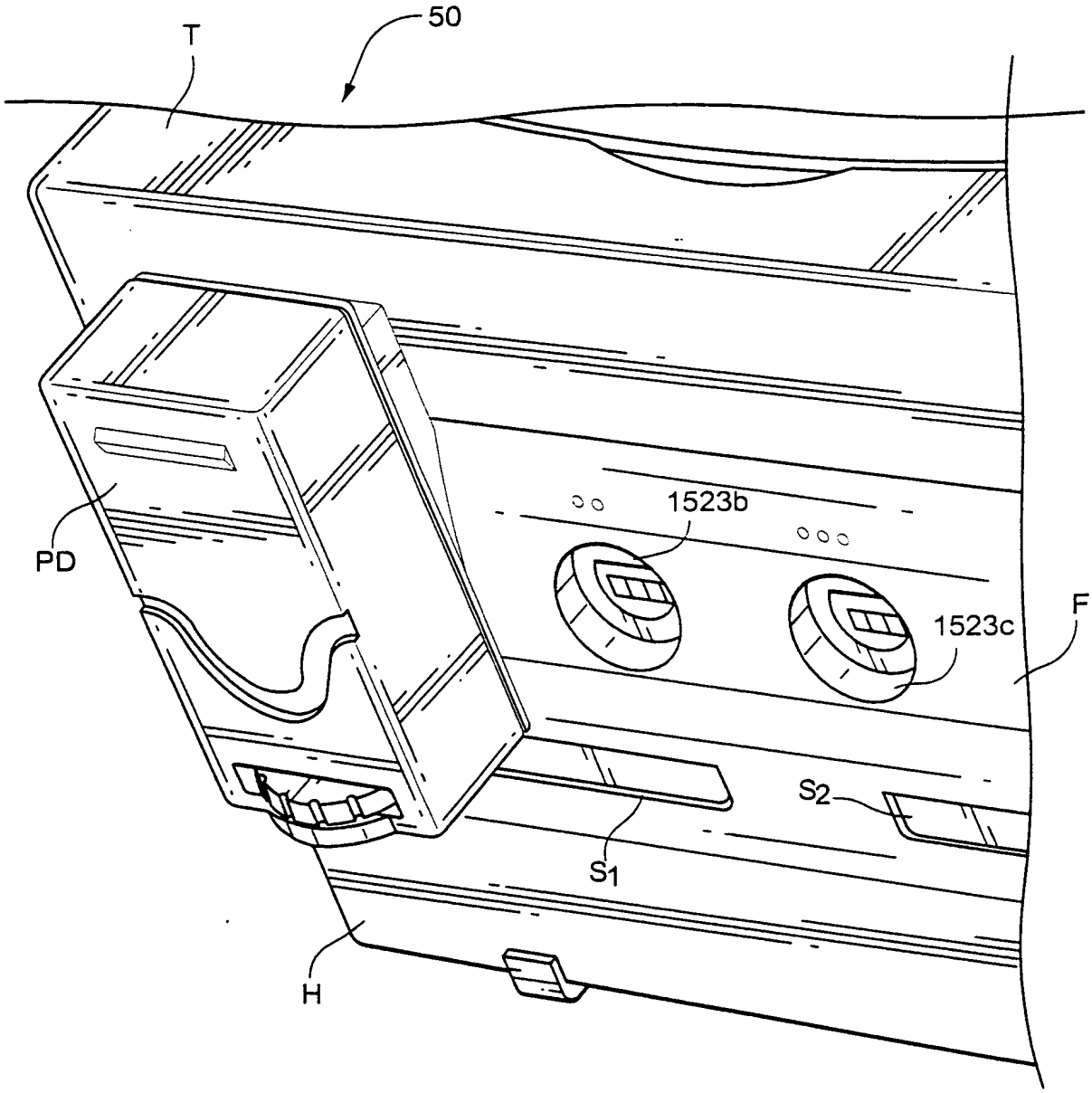



Fig. 24

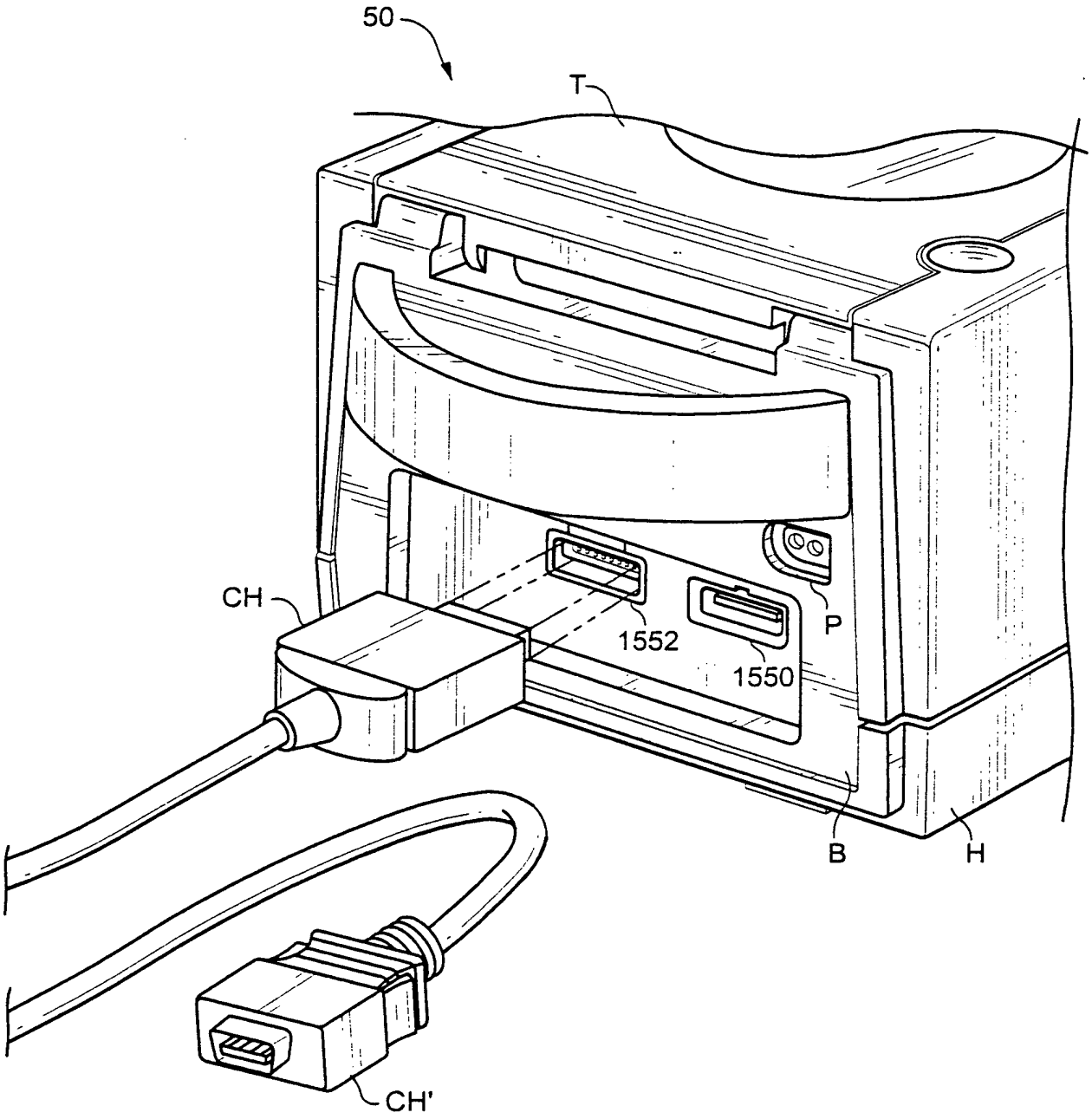



Fig. 25

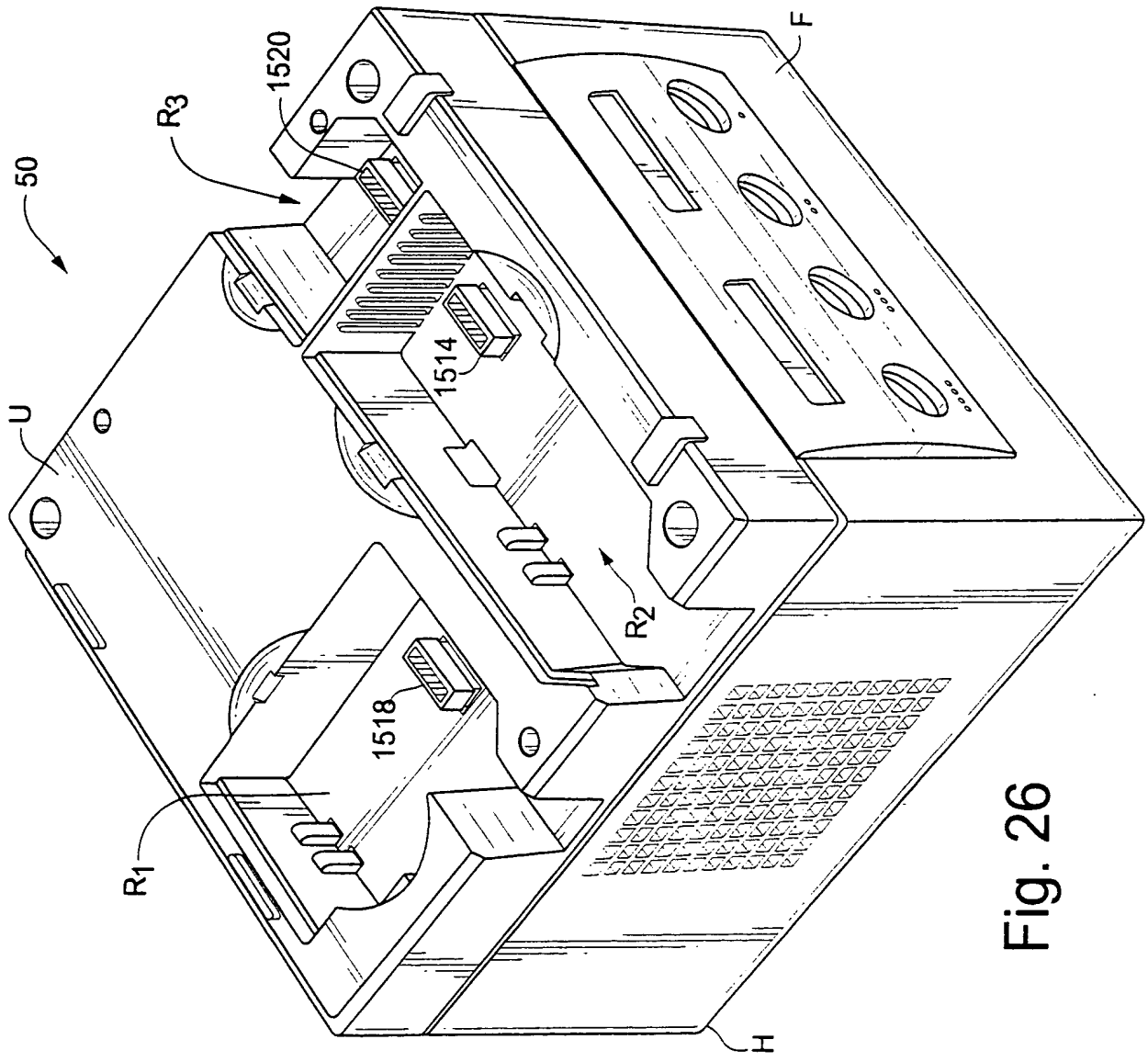



Fig. 26

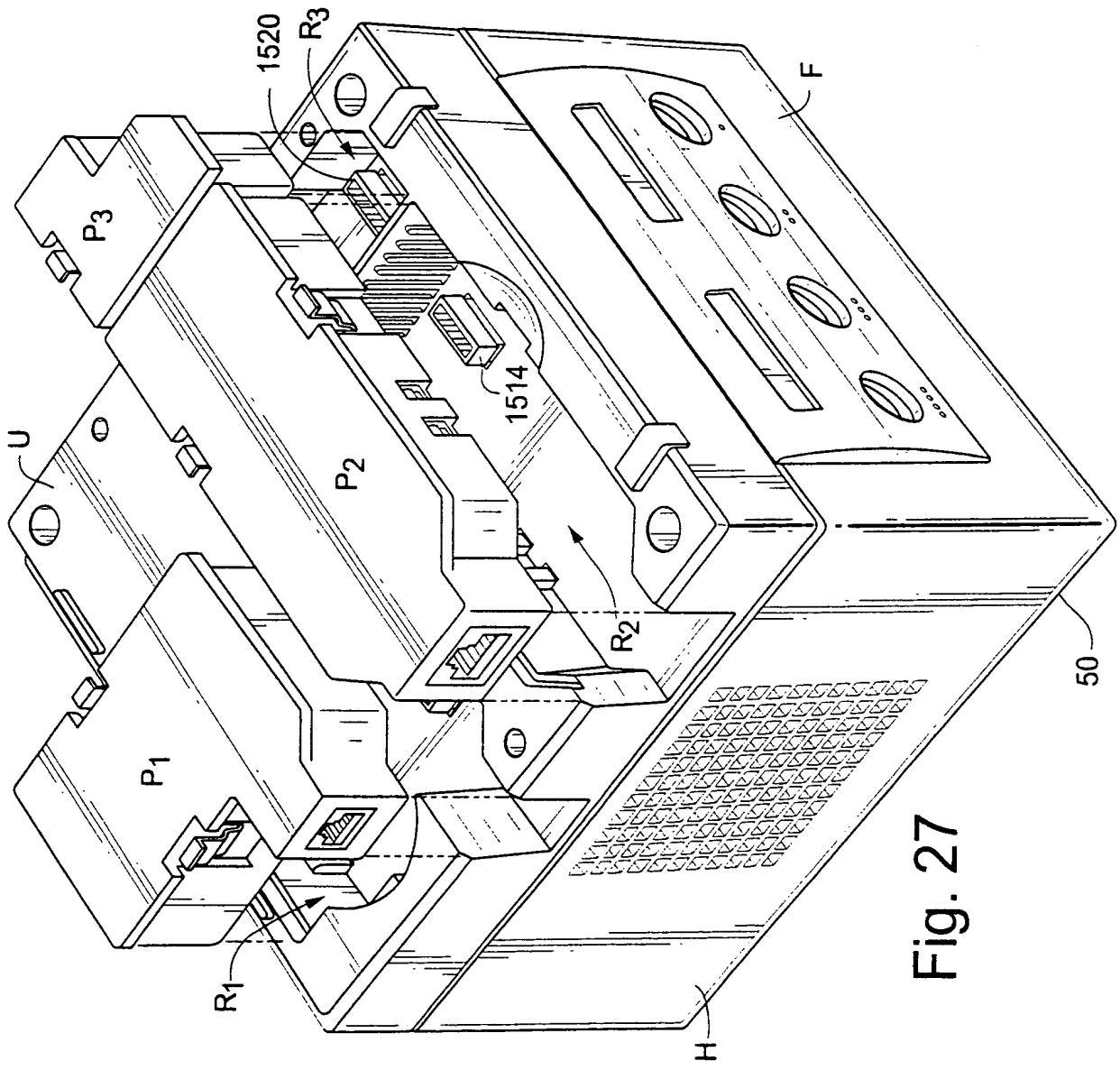



Fig. 27

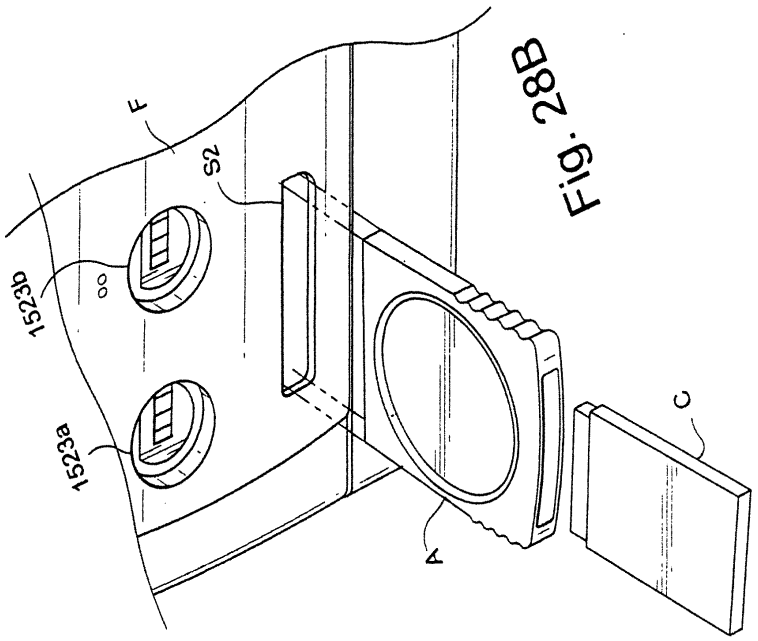



Fig. 28B

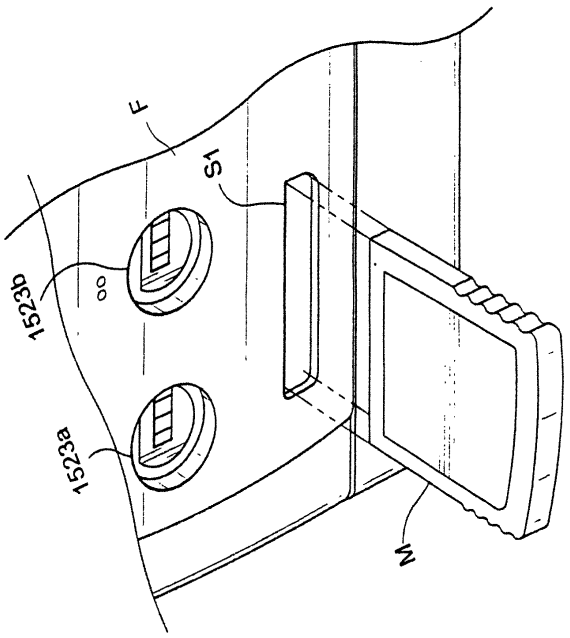



Fig. 28A

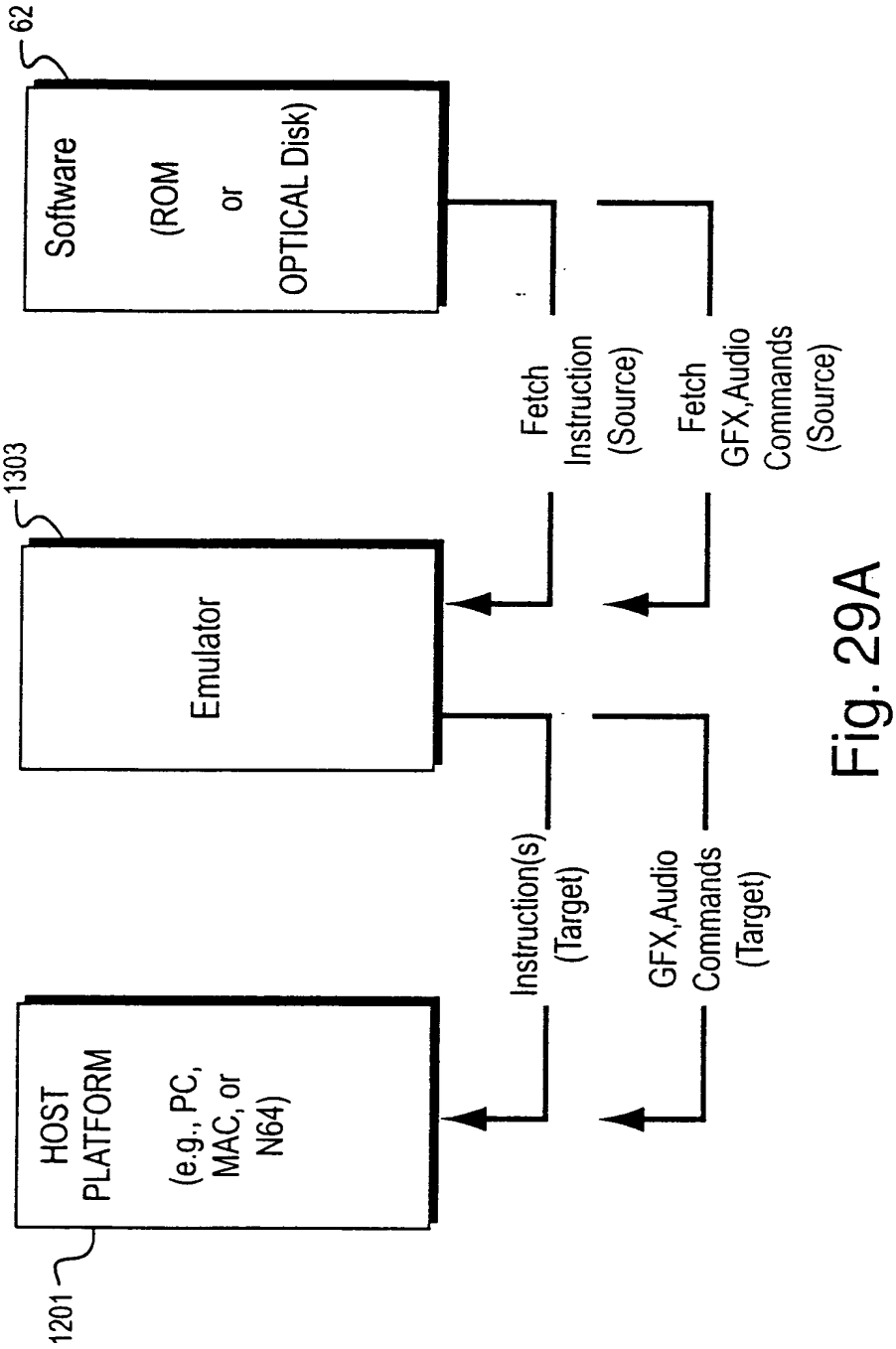

62
Software
(ROM
or
OPTICAL Disk)
1303
Emulator
1201
HOST
PLATFORM
(e.g., PC,
MAC, or
N64)
Fetch
Instruction
(Source)
Fetch
GFX,Audio
Commands
(Source)
Instruction(s)
(Target)
GFX,Audio
Commands
(Target)

Fig. 29A

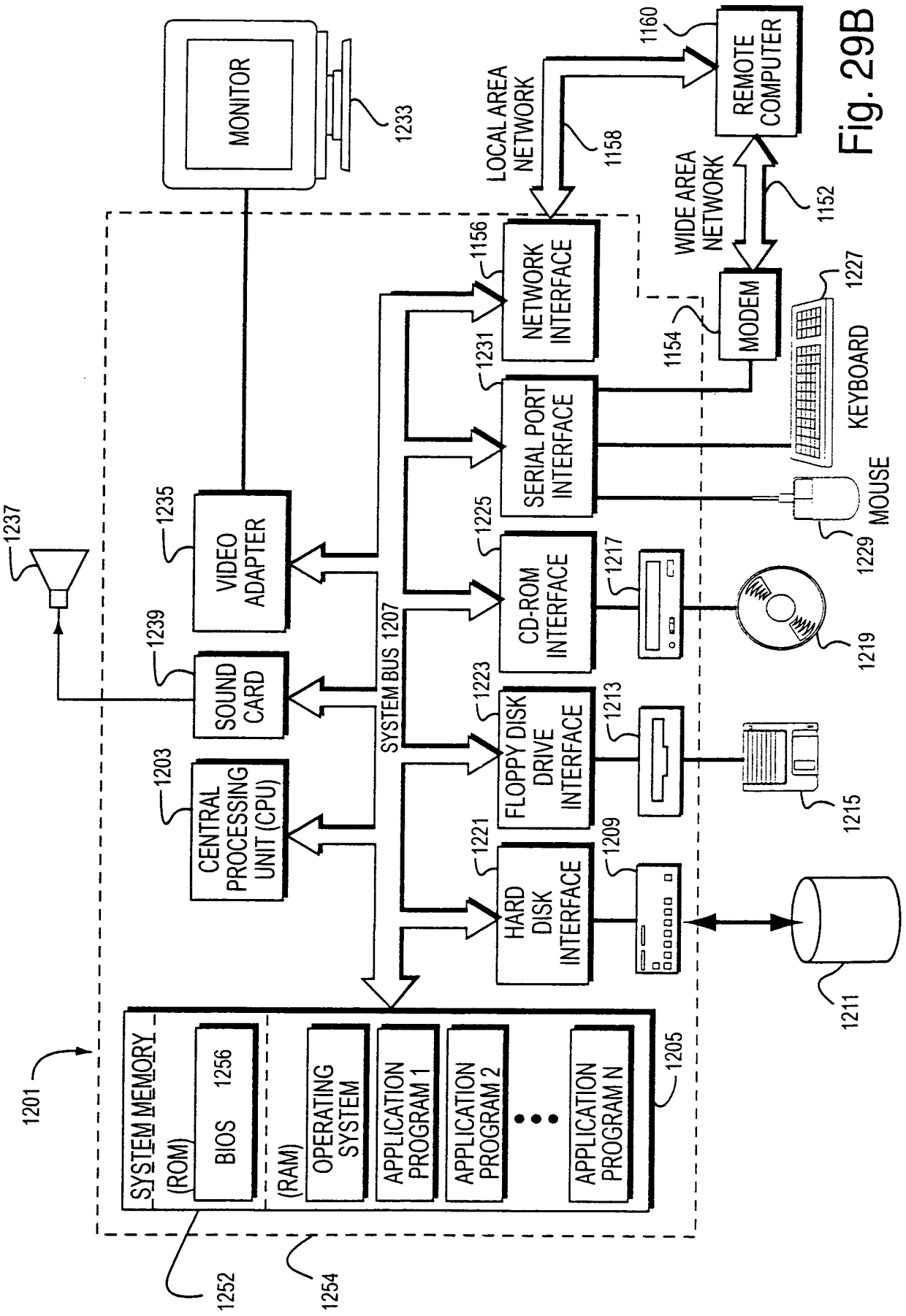

MONITOR
1233
LOCAL AREA NETWORK
1158
1160
REMOTE COMPUTER
WIDE AREA NETWORK
1152
1156
NETWORK INTERFACE
1231
SERIAL PORT INTERFACE
1154
MODEM
1227
KEYBOARD
MOUSE
1229
1225
CD-ROM INTERFACE
1217
1219
1223
FLOPPY DISK DRIVE INTERFACE
1213
1215
1221
HARD DISK INTERFACE
1209
1211
SYSTEM BUS 1207
1235
VIDEO ADAPTER
1237
1239
SOUND CARD
1203
CENTRAL PROCESSING UNIT (CPU)
1201
SYSTEM MEMORY
(ROM)
BIOS 1256
(RAM)
OPERATING SYSTEM
APPLICATION PROGRAM 1
APPLICATION PROGRAM 2
APPLICATION PROGRAM N
1205
1252
1254

Fig. 29B